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Design and realization On Board Data Handling for remote sensing payload of nanosatellite FPGA base

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Design and Realization On Board Data Handling for Remote Sensing Payload of Nanosatellite FPGA Based

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Abstract

The electronics and materials technology over the past decade provide new breakthroughs in the development of ICT (Information and Communication Technology) field one is on satellite technology. Currently, satellite has been getting development in miniaturizing dimension and components to the level of 1 kg weight. Nanosatellite is a class of satellites less than 10 kg in weight. One of the component subsystems that are in remote sensing payload nanosatellite which is contained within OBC (On-Board Computer) and in the application called OBDH (On Board Data Handling). The presence of the platform OBDH nanosatellite payload subsystem is very important, because to serve the flow of data from the camera and the transmitter. In this project, it will be designed and realized OBDH-based on FPGA (Field Programmable Gate Array). Because FPGA has many advantages over commonly used conventional microcontroller. In the development of space technology implementation for FPGA resistant to radiation effects in a parallel mechanism in the internal system that is ideal for future space applications, higher computational capability, low power consumption, small hardware size, and many others.

FPGA-based OBDH in this thesis are designed to set the process and control bits data input from the camera to the SDRAM and to the transmitter output from the SDRAM to be sent to the Ground Segment. Components are required as input the output information in the form of camera payload TCM 8240MD, internal SDRAM FPGA board. Communication used between the camera and FPGA with I2C bus protocol (Inter-IC). This FPGA will be encoded in VHDL language. Software used in a VHDL design is WebPack XILINX ISE, ModelSim, XSTOOLS Utilities. The execution and realization will be conducted in the supporters laboratory such as Digital Techniques and Microprocessor and Interfacing Laboratory. FPGA used is a Xilinx Spartan-200A XuLA with a maximum operating frequency of 384 MHz, because of the small dimension and the low power consumption and digital camera 1.3 Megapixels TCM 8240 that is capable with the Xula200 for performance in imaging. Going forward, the algorithm is programmed with VHDL language will be generated into the ASIC to strengthen and make it solid logic gates in the VHDL language in future space technology research.

Key words: FPGA, Xula-200, On-board Data Handling, VHDL, Remote Sensing Payload, nanosatellite and camera.

1. Introduction

Currently IT Telkom is developing nano satellites or nanosatelit for research purposes. Nanosatelit is one of a class of small satellites weighing less than 10 kg. Remote Sensing Payload is one of the subsystems that exist in nanosatelit. Payload subsystem serves to give an image that can be processed for purposes such as ship monitoring and tracking, border

monitoring, deforestation and so on. One of the subsystems within the component nanosatelit is On-Board Data Handling (OBDH) remote sensing payload. The presence OBDH the payload subsystem platform nanosatelit to serve the processing of data from cameras, camera control, error correction, and raw data delivery to the transmitter. FPGA (Field Programmable Gate Arrays) are able to perform its function as OBDH.

Field Programmable Gate Array (FPGA) has advantages as configured by the End User, and does not require the fabrication process, there is a solution that supports customized VLSI chips, being able to implement the logic circuit, instant manufacturring, very-low-cost prototype, the development of space technology for FPGA implementation resistant to the effects of radiation on parallel mechanisms in internal systems that are ideal for future space applications, programming brief for functions and capabilities equivalent to ASIC, and others. One of the problems of designing nanosatelit is power limitations arising from the dimensions and weight of a small nanosatelit. Power is required as the power supply is a maximum of 5.26 watts. With dimensions of space designed payload is 2 cm x 8 cm x 10 cm. OBDH is responsible for controlling the camera and control the flow of data bits from the camera to be sent to the transmitter if the data will be required, which has been stored in memory. Xula FPGA operating frequency is 200 MHz and 384 maximum mancai I2C protocol. Power input to be designed OBDH FPGA are 1.2 volts with a current consumption of 500 mA and FPGA board dimensions 51 mm x 25 mm.

2. Problem Formulation

In designing and making On-Board Data Handling (OBDH) there are some problems to be solved. Those issues are:

- How to make OBDH with fault tolerance (fault tolerance) is very minimal.
- How to make OBDH for camera control and data flow of the CMOS camera subsystem TCM8240MD are able to handle 15 frames per second.
- How the OBDH with base 200 Spartan 3A FPGA Xula the VHDL language according to the design specifications, the dimensions that can fit in the allocated space in the payload 10 x 8 x 2 cm with a power of less than 5.26 Watt.
- How to test OBDH realized to be compared with the design specifications.

3. Methode of solution

3.1. Power and Physical Constrain

In the design of the remote sensing payload nanosatelit in this research refers to the design of the national research program nanosatelit IiNUSAT-1 are assigned to retrieve and send data such as pictures or images to the ground station. In perancangannya, payload is certainly membutuhkan a controller or 'otak' yang responsible for controlling tasks tersebut. Pengiriman payload data from the camera must be sent to the transmitter with good quality at bit error is very small. It takes OBDH with payload dimensions according to the specifications nanosatelit IiNUSAT-1 is 2 cm x 8 cm x 10 cm and a maximum power of 5.26 watts. So dibuthkan OBDH dimensions and power of a small and inadequate specifications. Picture-1 design nanosatellite OBDH more details on the figure 3.1 below.

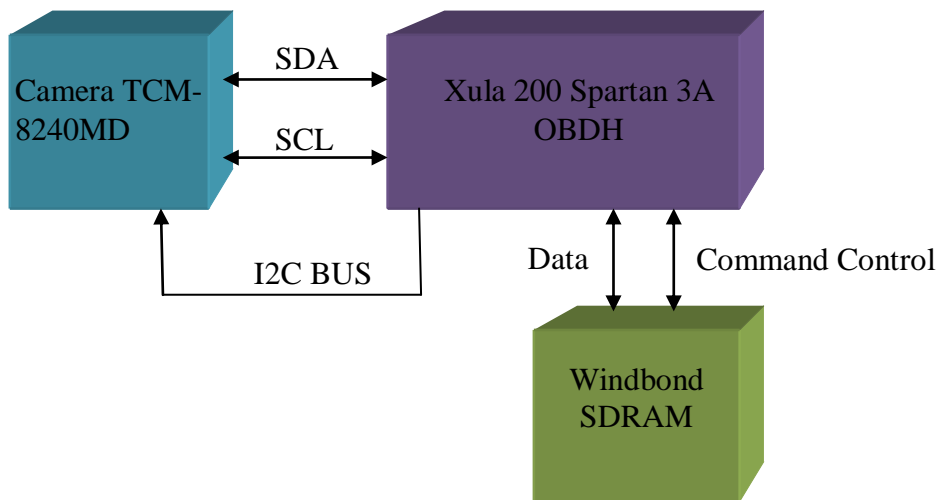


Figure 1. Diagram Block OBDH Payload Design

Here are the specifications of On-Board Data Handling specified:

- Power payload (maximum) : 5.26 Watt
- Consumption Current : 500 mA
- Power input (regulator) : 1.2 Volt - 3.3 Volt
- FPGA : Xilinx Family
- SDRAM : 128 Mbit, 2 Mbit Flash
- The total dimensions : <(70 cm x 70 cm)
- Frequency : 12 MHz oscillator, 384 MHz maximum operating frequency [10]

3.2. CMOS Camera TCM 8240 Toshiba

3.2.1 Device Description

TCM8240MD is an area color image sensor, at 1.3 Mega-pixels of array resolution (1300x 1040), incorporating a camera signal processor. The optical format is 1/3.3 inch of which small size is suitable for built in camera module application. Use of the CMOS process makes possible low power consumption operations. This sensor provides superb picture quality. This CMOS camera capable up to 15 fps frame rate for every resolution. Dual power supply are either 2.5 +/- 0.2V or 2.8 +/- 0.2V and 1.6 +/- .1V. Because of the temperature in space is very extreme, the camera has temperature between -20 to +60 degree C and storage operation temperature between -30 to +85 degeree C. The sensor in optical size is 1/3.3 insh optical format with 1300 (H) x 1040 (V) effective pixel numbers, but the output of pixel number is 1280 (H) x 1024 (V) maximum. This pixel pitch is 3.3 um x 3.3 um in square pixel. And the output image size from this camera is 4.29 mm(H) x 3.43 (V) in RGB or YUV format. This sensor is controlled by i2c bus in data and clock bus. [12]

3.2.2 Operation

TCM8240MD is a simple breakout board for 1300x1040 CMOS camera. It uses 6 MHz oscillator. The dif\gital camera use a VGA controller as an output to the monitor in our research. This TCM8240MD has a top module for camera controller to control the state machine of the camera and I2C controller. [12]



Figure 2. Breakout Camera TCM8240MD[12].

Pin Description

Table 1. Pin Description camera TCM8240MD

PIN No.	SYMBOL	I/O	DESCRIPTION
1	DOUT3	O	Data output
2	DOUT2	O	Data output
3	DOUT1	O	Data output
4	DOUT0	O	Data output (LSB)
5	GND		GND
6	PVDD	I	Power supply 2.8+/-0.2V or 2.5+/-0.2V
7	RESET	I	Reset pulse to initialize
8	SCL	I	Clock for I2C bus
9	GND		GND
10	SDA	I/O	Data for I2C bus
11	GND		GND
12	DVDD	I	Power supply 1.6+/-0.1V
13	EXTCLK	I	External clock input
14	STROBE	O	Trigger pulse for flash strobe
15	HBLK	O	Horizontal data blanking period
16	VBLK	O	Vertical data blanking period
17	GND		GND
18	IOVDD	I	Power supply 2.8+/-0.2V or 2.5+/-0.2V
19	DCLK	O	Clock for output data
20	GND		GND
21	DOUT7	O	Data output (MSB)
22	DOUT6	O	Data output
23	DOUT5	O	Data output
24	DOUT4	O	Data output

This camera will be control by the camera controller in FPGA as OBDH that is connected with the I2C SDA and SCL line. The capturing of the camera is operated by those two wires, that manage the 8 bit data and clock cycle in the FPGA. Each port is connected to the Xula200 Board, and will be mapped by the VHDL port map design. And the clock frequency between the camera clock and the FPGA is the same clock, it uses 6 MHz in the camera.

3.3. SDRAM Windbond W9812G6JH Memory

3.3.1 Memory Organization Capacity and Interface

Memory W9812G6JH is high speed synchronous dynamic random access memory (SDRAM), organized as 2.097.152 words x 4 banks x 16 bits. This memory delivers a data bandwidth of up to 200M words per second. For different application, it is sorted into the following speed grades : -5/-6/-6I/-6A and -75. This memory is ideal for main memory in high performance applications. It has 3.3V +/- 0.3V for power supply and it is up to 200MHz for clock frequency and need 2 mA in current consumpt

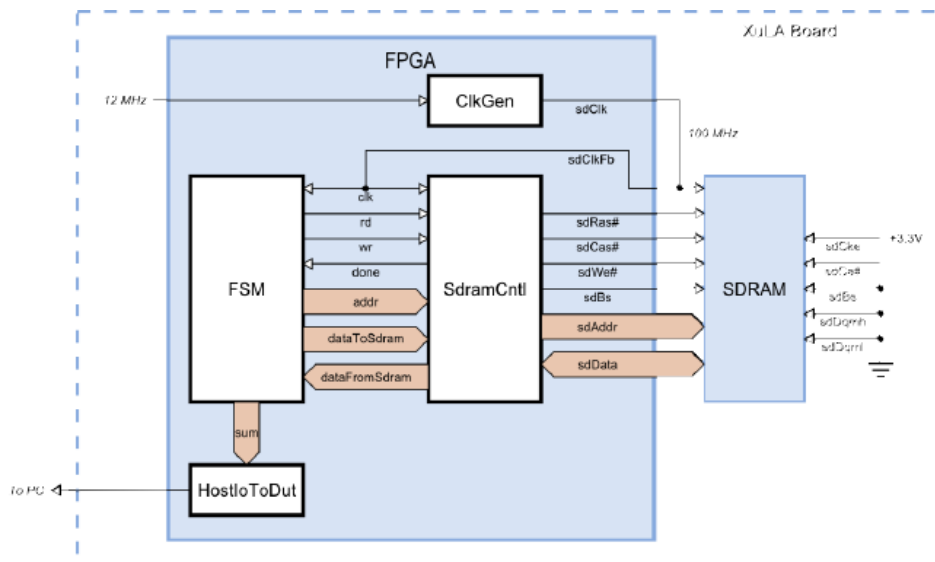


Figure 3. Diagram Block of SDRAM in Xula200 [10]

3.3.2 Memory Operation

The SDRAM controller module supports several modes of operation, but I'll use it here in its simplest and lowest-performance form to do non-pipelined reads and writes of SDRAM. The timing waveforms for a non-pipelined read operation are shown below. These assume the read operation accesses a memory location in the currently active bank and row of the SDRAM. The sequence of actions is:

Cycle 1: The SDRAM address is applied and the read control signal is driven high. The address and read control must be held stable until the done signal goes high.

Cycle 2: The column address is output on the pins that go to the SDRAM chip and the SDRAM control signals are set to initiate a read operation.

Cycle 3: The SDRAM initiates a read of the given column address on the rising clock edge.

Cycle 4: The SDRAM waits for the data to arrive from the given address.

Cycle 5: The data from the SDRAM arrives sometime during this cycle and is guaranteed to be stable by the end of the cycle.

Cycle 6: The data from the SDRAM is clocked into a register on the rising clock edge. The done signal goes high to signal the host-side logic that the data is available on the dataFromRam bus. The read control must be lowered before the next rising clock edge or else another read operation will be initiated.

Cycle 7: The done signal goes low again but the output data remains stable until another read operation is completed.

To operate the capable one, it uses up to 100 MHz clock frequency. The clock generator module multiplies the 12 MHz input clock by 25/3 to create the 100 MHz clock that is output to the SDRAM. The 100 MHz clock also re-enters the FPGA and becomes the master clock for all the rest of the FPGA circuitry.

The memory area in this SDRAM is 2112 bytes for example, it means that 2048 bytes of data and 64 bytes of spare area. 1 block of memory has 64 pages.

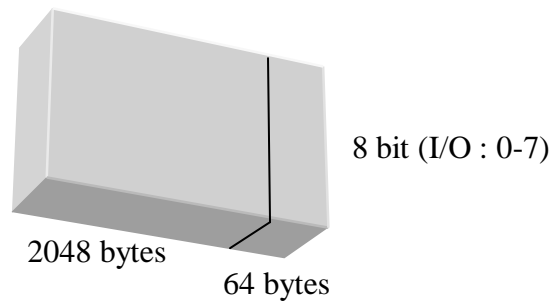


Figure 4. Part of detail memory [14]

1 pages = (2048 + 64) bytes

1 block = (2048 + 64) x 64 = 135.168 bytes

1 device = (2048 + 64) x 64 x 4096 = 553.648.128 bytes

3.4. Xilinx Xula 200 Spartan 3A

3.4.1 Spesification and Design Xula 200 Spartan 3A

To do the design according to the specifications above as the control processor and the data is Xula-200 FPGA Spartan 3A FPGA due to the small dimensions and specifications are 51 mm x 25 mm with a current consumption of 500 mA. The design of the processor and control data will use the language VHSIC Hardware Description Language (VHDL) and data transmission system using the First In First Out (FIFO). More details Xula board FPGA Spartan 3A-200 are as follows.

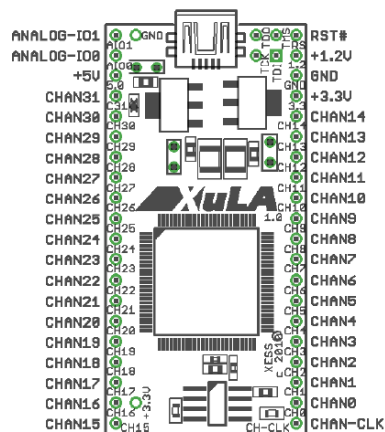


Figure 5. Sightings of Xula Spartan 3A-200 [10]

From the datasheet Xula-200 FPGA Spartan 3A are as follows.

- a. Power input (regulator): 1.2 Volt / 3.3 Volt
- b. Microcontroller: PIC 18F14K50
- c. FPGA: Xilinx Spartan 3A XC3S200A, 200,000-gate FPGA
- d. SDRAM: 128 Mbit, 2 Mbit Flash
- e. Frequency: 12 MHz oscillator 384 MHz maximum operating frequency

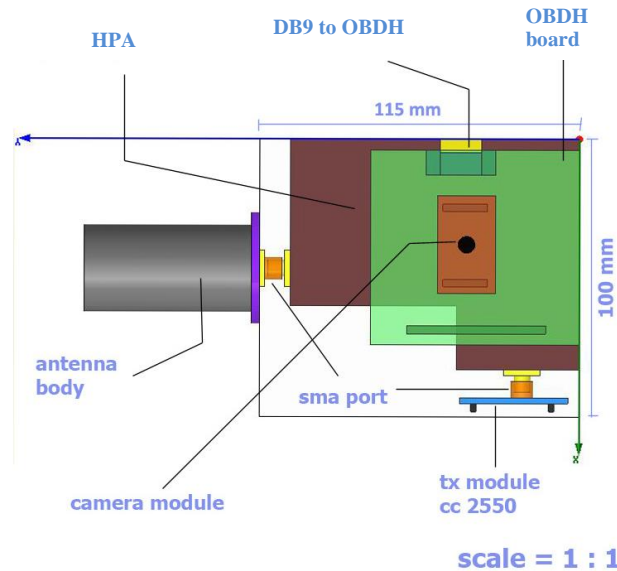


Figure 6. Payload of Nanosatellite module Sightings.

The module design above is a module that design to make a profile and simulate the dimension in payload nanosatellite. They are integrated in a modul , there are camera, OBDH, Transmitter, HPA and antenna modul.

3.5. Communication Methode

3.5.1 I2C communication

I2C bus physically consists of 2 active wire and a ground connection. The two active wires are both SDA and SCL are bidirectional. SDA (Serial Data line), SCL (Serial Clock line) both of which can be connected to other devices or multiple devices, eg an LCD driver, memory, camera module controller, ASIC, etc.. Each device driver can be a receiver and transmitter depending on its function. I2C is a multimaster bus, which means that more than one IC can initiate a data transfer interconnected and depend on the master bus. Example of

the diagram below, the FPGA will send the data to any one receiver (with Master-Slave mode)

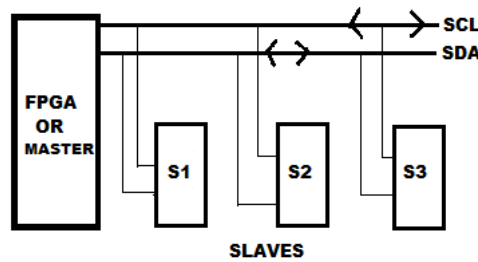


Figure 7. Block Diagram of I2C Master Slave.

The caption is as follows:

1. Master / FPGA will give a signal issue / START condition.
 2. Condition as a trigger signal to all slave.
 3. Slave understand the data flow in the data bus, so the address of the slave / device (camera) to be accessed, which in accordance access, read / write operation.
 4. If it does not fit then it will wait till the bus, issued a STOP condition.
 5. If the addresses match, the chip / device / slave will respond with ACK.
 6. Once Master / FPGA receives ACK signal from slave that will begin the process of Transmit and receive DATA. In such cases, FPGA / Master will send DATA (8 bits) after receiving the ACK.
 7. After all DATA completion, and FPGA / Master member will issue a STOP condition.
- So the statuses in this mode is START, ADDRESS, WRITE / READ, ACK, DATA, STOP.

S	ADD 7 BITS	S	ACK	DATA 8 BITS	ACK	P
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Figure 8. The composition of the signal on the I2C status

Master/slave state machine

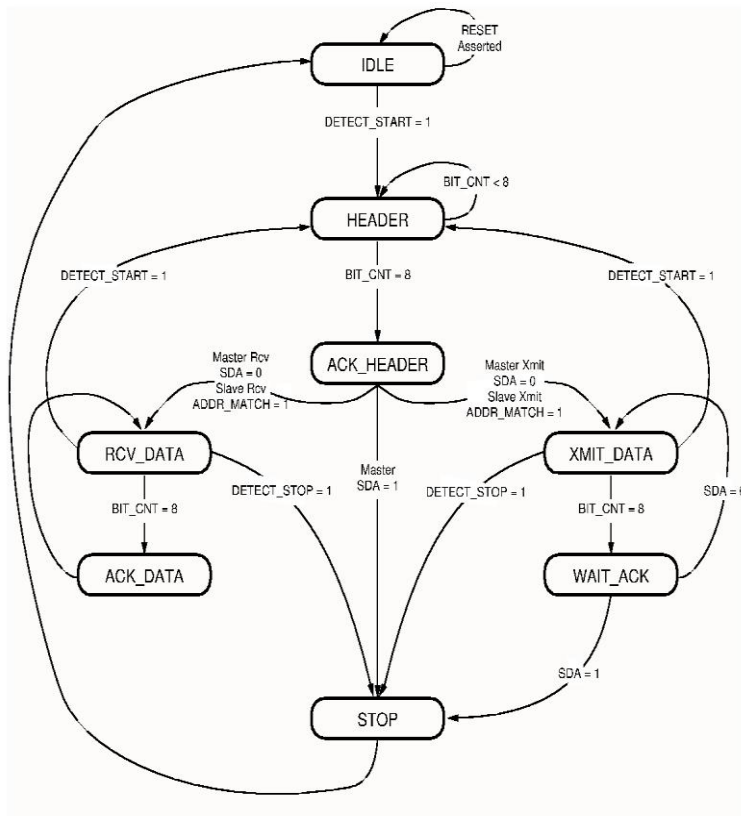


Figure 9. Flow chart master slave reference[5]

- **I2C Controller**

I2C is a serial data bus protocol which only has two bus signals, the SCL and SDA bidirectional. The bidirectional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between the camera and FPGA as On-board Data Handling. Devices controlling the buses are called as Master.

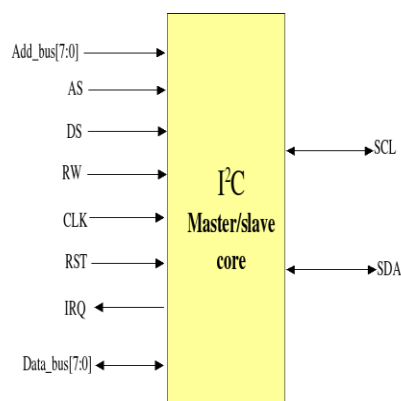


Figure 10. Pin interface of I2C [5]

Master is responsible for generation of bus control and synchronizing signals. Slave just follow the Master. It has two state machines, first is the main state machine which is same for either master or slave, while second is responsible for generating clock signal in master mode. These state machines have been interface with a module which is used for decoding the commands from I2C controller, processor in On-board Data handling (Xula200 FPGA). The module is actually interfaces with i2c module in the processor top module. By footprint on the signal ports I2C Controller is shown below.

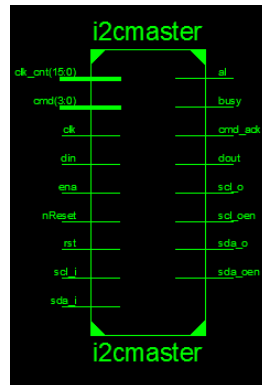


Figure 11. I2C master port mapping

4. Result and Discussion

4.1 Sistem Minimum for Integrating Camera and OBDH FPGA

In optimizing the integration between the camera module and the FPGA Xula200 TCM8240MD board, the need for a module or a minimum system that will integrate the two modules and also modul additional modules to make a simple interfacing between OBDH and camera modul, as shown below.

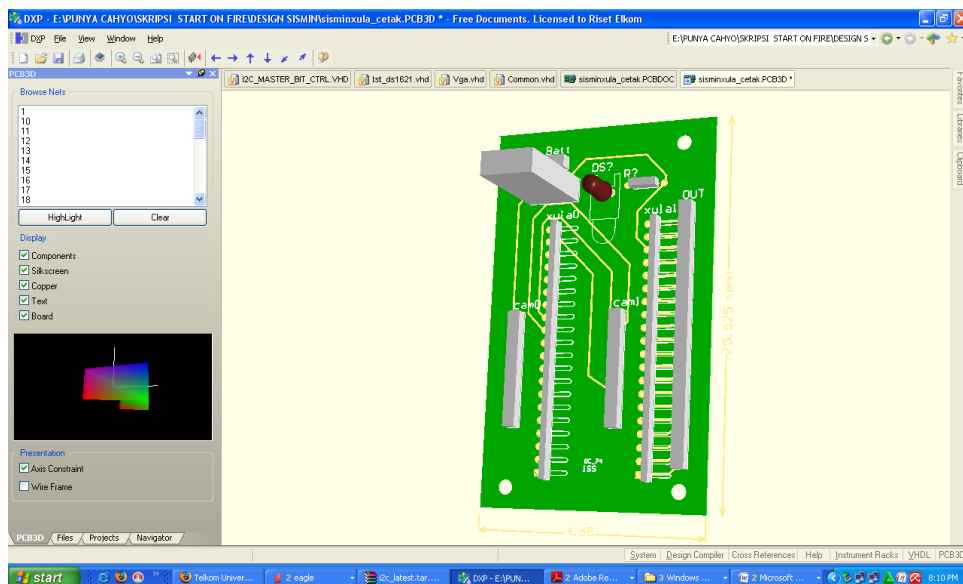


Figure 12. The appearance of the 3D minimum system design of DXP Software

Memory capacity and image data allocation

Xula200 Spartan 3A FPGA board has SDRAM and NAND Flash memory. NAND Flash is 2 Mbit = 250kb, and SDRAM (volatile) is 128 Mbit = 16 MByte.

There are two possibilities for calculating the image size from the camera to the memory. TCM8240MDS (1300 x 1040 pixels), can be calculated as below

1. For the output data rate is 32 bit/pixel. The image size is $1300 \times 1040 \times 32 \text{ bit} = 43264000 \text{ bit/ image} = 5,408 \text{ MB/ image}$. So the image allocated in S\memory is $= 5,408 \text{ MB/image} = 16 \text{ MB/ } 5,408 \text{ MB} = 3 \text{ images}$.
2. For the output data rate is 10 bit/ pixel. The image size is $1300 \times 1040 \times 10 \text{ bit} = 13520000 \text{ bit/image} = 1,69 \text{ MB/ image}$. So it be allocated in $16 \text{ MB} / 1,69 \text{ MB} = 9 \text{ images}$.

So we can see, the image that can be allocated in this memory SDRAM is maximum 9 images for 10 bit/pixel data rate. And this camera TCM8240MD has 15 fps for frame rate. So it supports the high rate.

Power Design

1. Xula200 Spartan 3A

This FPGA has 5 volt and 500 mA current consumption.

Power consumption, $P = V \cdot I = 5\text{V} \times 500\text{mA} = 2500 \text{ mWatt}$. But, this FPGA can regulate to 3.3V and 1.2V. So it can be 1650mWatt and 600 mWatt.

2. Camera TCM8240MD

The camera has 1.5Volt and 180mA cureent. So, the power consumption is $P = V \cdot I = 1.5\text{V} \times 180\text{mA} = 270 \text{ mWatt}$.

3. Memory

The memory has two part, there are SDRAM and NAND Flash. For the SDRAM, it has 3.3V voltage regulator and 2mA current. So the Power consumption is $P = V \cdot I = 3.3\text{V} \times 2 \text{ mA} = 6.6\text{mWatt}$.

And for the NAND Flash, it has 3.6V voltage and 4mA current. The power consumption is $P = V \cdot I = 3.6\text{V} \times 4 \text{ mA} = 14.4\text{mWatt}$.

The total power memory is $P = 6.6\text{mW} + 14.4\text{mW} = 21\text{mWatt}$.

From all calculating above it can be conclude, the total power for this OBDH and camera system is $2500\text{mW} + 270\text{mW} + 21 \text{ mW} = 2791\text{MwATT} = \mathbf{2.791 \text{ Watt}}$. The constrain of power for this system is 5.26 Watt for all payload. So it is possible to pass the power constrain.

Clock Generation

Xula200 has a DCM to manage the clocking to generate, from 12 MHz frequency clock then manage it into 50MHz like the smilation from Logic Analyzer figure below. But, the master clock is up to 384MHz. It is capable to the speed for transferring the data and interfacing with the other modul.

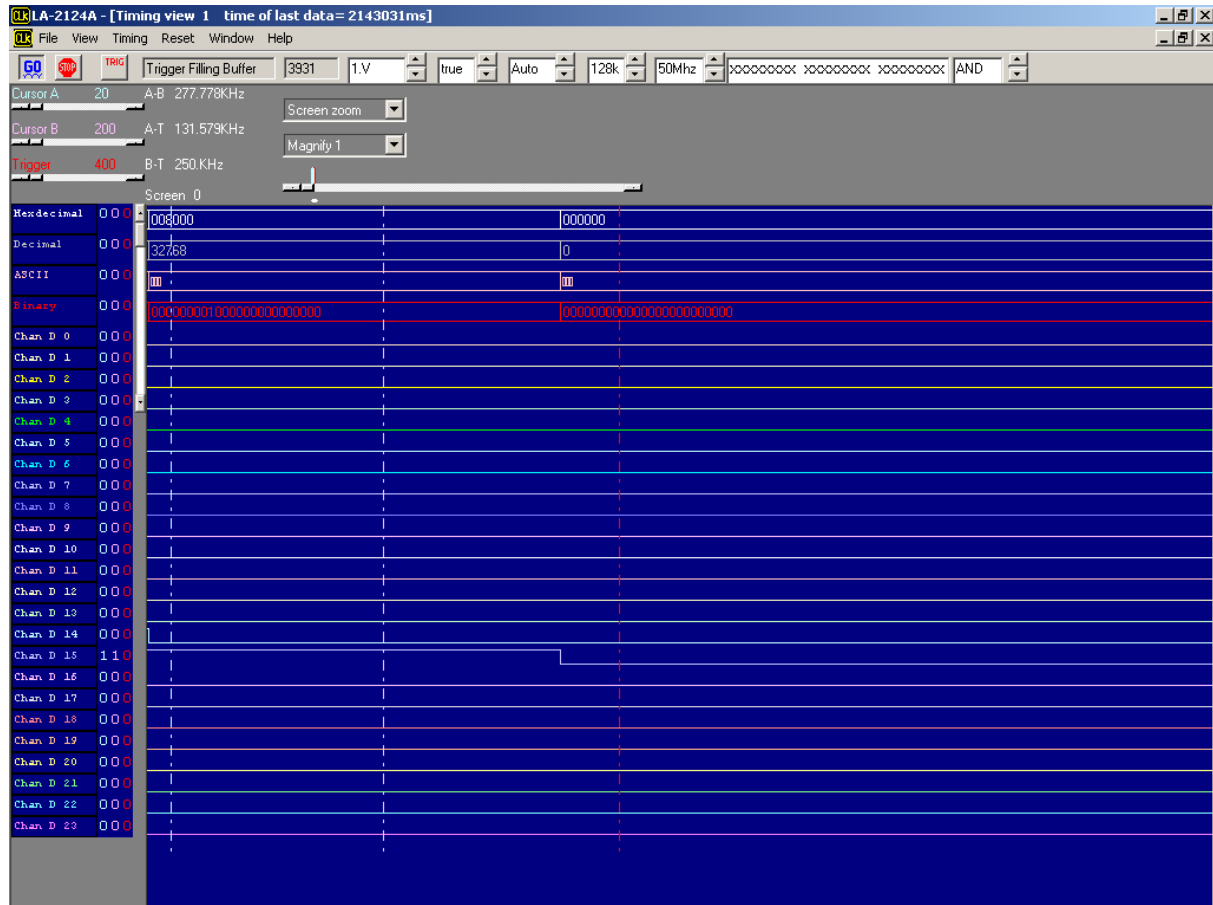


Figure 13. Clock generation test from Logic Analyzer

5. Conclusion and Further Work

The design and calculating of OBDH module belong to camera provides the capability for the power and dimension constrain in this case. Nanosatellite that provides 2 x 8 x10 cm in length is very challenging. OBDH module and camera module has to be integrated in a system minimum I called, it can get the optimal performance of OBDH system.

The simulation provides a performance for each block in OBDH system, such as camera controller, SDRAM controller, and the top level.

6. Acknowledgement

This research is an ongoing research and will develop further. Remote sensing payload is an excellent research in Telkom Institute of Technology today. And a roadmap to the future of the Telkom Institute of Technology research team will be focused to advance Remote Sensing Payload and will lead ITT-Sat, the nanosatellite research team made by Telkom Institute of Technology itself.

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