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Analysis of parallel connected Fibonacci switched capacitor converter

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Abstract

Switched capacitor converter (SCC) is a power converter without magnetic components. SCCs have been used in various portable electric products such as flash memories and energy harvesting systems. Conservative SCCs separately charge and discharge their output capacitors during one operating cycle. This operation reduces power efficiencies and increases output ripple voltages. To improve this problem, a parallel connected Fibonacci SCC (PFSCC) was suggested. The symmetric structure of the PFSCC can lead to its better output performance. As a preliminary stage to design a hardware and a controller for the PFSCC, this paper performs an analysis of the PFSCC to derive parameters such as its optimized capacitance and power stage transfer function. Also, simulations and comparisons with 4 different SCCs are conducted to verify its performance.

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Keywords: Switched capacitor converter; Symmetric structure; Component optimizing; Circuit modeling

1. Introduction

Switched capacitor converter (SCC) is a type of power converters. The SCC consists of semiconductor switches and capacitors without magnetic components such as inductors or transformers. This leads to reduction in the weight and size. Therefore, SCCs are usually used for portable devices like flash memories, energy harvesting systems and so on Forouzesh et al. [1]. There are several kinds of widely used SCCs such as Fibonacci type SCC (FSCC) [2], switched capacitor voltage multiplier (SCVM) [3], Dickson SCC [4] and series–parallel SCC [5]. These types of SCCs separately charge and discharge their output capacitors during their one operation cycle. This causes SCCs to increase the output ripple voltages and the capacitances of their output capacitors, and to reduce the power efficiencies as well. To improve those drawbacks, we suggested a parallel connected Fibonacci SCC (PFSCC) in previous study [6]. The symmetric structure of the PFSCC can improve its performance compared to the normal FSCC. However, the study [6] was not enough to implement a real hardware realization of the FSCC. The reason of this is because it was not performed in the past study to compare the PFSCC with more different types of SCCs in order to verify its performance and to analyze it with its switching frequency so as to design its controller. In

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this paper, a comparative study with other SCCs and a theoretical analysis of the PFSCC in its stable state are implemented as a preliminary study to design a hardware and a controller for the PFSCC. To analyze the PFSCC, four-terminal equivalent (FE) model [6] is utilized to derive its conversion ratio and output impedance. Although the modeling of slow and fast switching limit impedance in the study [7] is more accurate than the FE model, there is an assumption in the modeling that a targeted SCC has only 50% duty ratio of its switch-on and off time for its switching period. Unlike that, it is possible to regulate the duty ratio in the FE model. In the study [8], capacitor ampere-second balance transient calculation (CASBTC) modeling method is even more precise than the model of Seeman and Sanders [7] but CASBTC is performed based on differential equations with every single capacitor capacitance in the targeted converter. This requires more tedious and complex expressions for parameters of any SCCs when they are constructed with tens capacitors and switches. In this paper, the PFSCC is analyzed based on charged and discharged charge amounts in capacitors of the PFSCC during one operating cycle. This method leads to concise expressions compared with two abovementioned analysis methods. Also, sizing capacitance of capacitors in the PFSCC and deriving power stage transfer function of it can be performed. Concretely, conversion ratio, output impedance, capacitance sizing and power stage transfer function of the PFSCC are theoretically derived by using two analysis methods of the FE model and the charge amount calculation.

The remainder of this paper is divided as follows. Section 2 introduces the circuit configuration of the PFSCC. In Section 3, the PFSCC is theoretically analyzed to derive parameters. Section 4 describes simulations and comparisons with 4 different SCCs. In Section 5, we discuss a conclusion and a future study.

2. Converter topology

2.1. PFSCC

Fig. 1 illustrates a PFSCC consisting of two normal FSCCs connected in parallel. This parallel structure can continuously provide boosted voltages to the output capacitor, while a normal FSCC charges and discharges it at each half operating cycle, respectively. Switches of the PFSCC are operated by a switching rule. The switching rule is that S1 switches are on and S2 switches are off when the PFSCC is in state-1, and S1 switches are off and S2 switches are on when it is in state-2. This operation and structure reduce the capacitance of the output capacitor than that of the normal FSCC, which also indicates that it helps the PFSCC generate its output voltage with smaller output ripple voltages than that of the normal one [6].

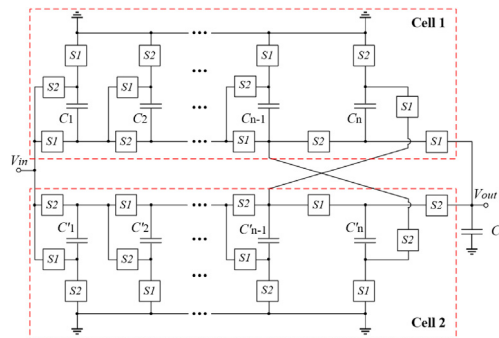


Fig. 1. Circuit configuration of the PFSCC.

2.2. The operation of PFSCC

The PFSCC has two IECs (instantaneous equivalent circuits) during one operating cycle. Fig. 2 illustrates the IECs at the conversion ratio of 4 times. In the switching rule, n th capacitor in each stage of each cell is charged up to the sum of $(n-1)$ th and $(n-2)$ th capacitors' voltage, where $n > 2$. When $n = 1, 2$, the first and second capacitors (C_1 and C_2 , and C'_1 and C'_2) are charged up to 1 and 2 times V_{in} , respectively. In both cases, the n th capacitors are connected in series so that the PFSCC can generate 2 times higher output voltage than that of the normal FSCC.

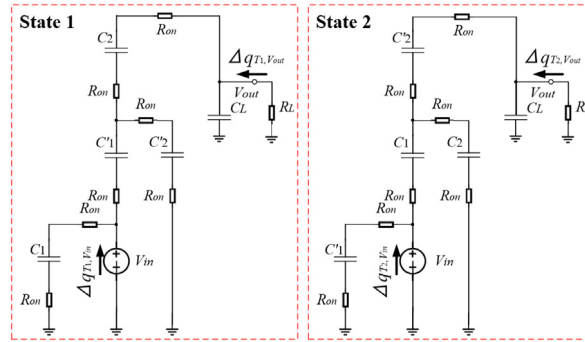


Fig. 2. IECs of the PFSCC at the conversion ratio of 4 times.

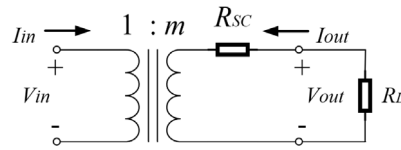


Fig. 3. The four terminal equivalent model.

3. Theoretical analysis and capacitor optimization

3.1. FE model

The PFSCC is analyzed based on the four-terminal equivalent circuit model in Fig. 3. In Fig. 3, I_{in} , I_{out} , V_{in} , V_{out} , and m are the input and output average current, the input and output average voltage and the conversion ratio of a modeled converter, respectively. R_{SC} and R_L are the switched capacitor resistor (output resistor or impedance) and the load resistor of it. This modeling is performed with the conversion ratio of 4 times.

During operating states (state-1 and 2), charged and discharged charge amounts of all capacitors are the same as shown as (1).

$$\Delta q_{T1}^y = -\Delta q_{T2}^y, \quad \Delta k_{T1}^y = -\Delta k_{T2}^y, \quad (1)$$

where Δq_{T1}^y , Δk_{T1}^y , Δq_{T2}^y and Δk_{T2}^y ($1 \leq y \leq n$) are the charge amounts of the y th capacitor in y th stage of cell-1 and 2 at state-1 and 2, respectively.

By setting the 50% duty ratio of each operating state, the operating period, T , of the PFSCC is given as (2).

$$T = \sum_{i=1}^2 T_i \text{ and } T_1 = T_2 = T/2. \quad (2)$$

By applying KCL to IECs in Fig. 2, the relations of the input and output source and capacitors of PFSCC are given as (3) at state-1 and 2, respectively.

$$\Delta q_{T1,V_{in}} = \Delta q_{T1}^1 - \Delta k_{T1}^1, \quad \Delta q_{T1,V_{out}} = \Delta q_{T1}^L + \Delta q_{T1}^2, \quad \Delta q_{T2,V_{in}} = \Delta k_{T2}^1 - \Delta q_{T2}^1, \quad \Delta q_{T2,V_{out}} = \Delta q_{T2}^L - \Delta q_{T2}^2, \quad (3)$$

where $\Delta q_{T1,V_{in}}$ and $\Delta q_{T1,V_{out}}$ are the charge amounts of input and output source and Δq_{Ti}^L is the charge amount of the output capacitor at state-1 and 2, ($i = 1$ and 2).

By substituting (1) into (3), the relation of average input and output current for one operating cycle, I_{in} and I_{out} , are given as (4). Therefore, the conversion ratio of PFSCC, m , is 4.

$$I_{in} = -4I_{out}. \quad (4)$$

To calculate R_{SC} , the consumed energy during one operating cycle is given as (5). Because it has the symmetric IECs, the consumed energy, W_{T1} and W_{T2} , are the same and W_T is obtained. From this, R_{SC} is derived as $16R_{on}$.

$$W_{T1} = W_{T2} = \{(4R_{on})/T\} (\Delta q_{T1}^{out})^2, \quad W_T = \{(16R_{on})/T\} (\Delta q_{Vout})^2. \tag{5}$$

By using derived parameters, the output voltage and efficiency, η , can be calculated as (6).

$$V_{out} = \eta V_{in} = \{R_{SC}/(R_L + R_{SC})\} V_{in}. \tag{6}$$

3.2. Capacitor optimization

To determine sizes of capacitors, we assume that all charged energy in flying capacitors can be transferred into the output capacitor without any loss. With this assumption, the difference between the charged and discharged charge amounts in flying capacitors should be the same as the total charge amount of the output capacitor during one operation cycle, which is expressed as (7).

$$C_f \left(\frac{3}{2}\right) V_{out} - 2C_f (V_{out} - V_{in}) = C_L \Delta V_{out}, \tag{7}$$

where ΔV_{out} is the ripple voltage of the output and C_f and C_L are the capacitances of the flying capacitors and the output capacitor.

If the ripple voltage is much smaller than the output voltage, the transferred energy, $E_{transfer}$, into the output capacitor can be expressed as (8). $E_{transfer}$ should be the same as the consumed energy by the load.

$$E_{transfer} = C_L V_{out} \Delta V_{out} = \frac{(V_{out})^2}{R_L} \cdot \frac{1}{f}. \tag{8}$$

where f is the frequency of the operating cycle.

By combining (7) and (8), the capacitances of the flying capacitors and the output capacitor can be optimized as (9) and, respectively.

$$C_f = V_{out} / \{R_L \cdot f \cdot (2V_{in} - V_{out})\}, \quad C_L = V_{out} / (R_L \cdot f \cdot \Delta V_{out}) \tag{9}$$

3.3. Power stage transfer function

With consideration of a digital control, the PFSCC is modeled in z-domain to obtain its power stage transfer function. First, At $(n - 1)T$, the total charged charges in all capacitors, Q_{charge} , are derived and expressed as (10).

$$Q_{charge} ((n - 1) T) = \left(\frac{3}{2}C_f + C_L\right) V_{out} ((n - 1) T). \tag{10}$$

At nT , the discharged charges in all capacitors, Q_{disch} , are calculated as (11)

$$Q_{disch} (nT) = 2C_f (V_{out} (nT) - V_{in} (nT)) + C_L V_{out} (nT). \tag{11}$$

The output current during one operating cycle, T , should be equal to the difference between the charged and discharged charges divided by T , which is given as (12).

$$\frac{(Q_{charge} ((n - 1) T) - Q_{disch} (nT))}{T} = \frac{(V_{out} ((n - 1) T) + V_{out} (nT))}{R_L}. \tag{12}$$

By substituting (10) and (11) into (12) and transferring it on z-domain, the power stage transfer function of the PFSCC is derived as (13).

$$\frac{V_{out}}{V_{in}} = \frac{2C_f}{\left[\left\{-\frac{3}{2}C_f - 2C_L + (T/R_L)\right\} + \left\{2C_f + 2C_L + (T/R_L)\right\}\right]} z^{-1}. \tag{13}$$

4. Simulation and comparison

To compare the PFSCC with 4 SCCs (normal Fibonacci [2], Dickson [4], SCVM [3] and series–parallel type [5]), the converters are simulated with the conditions as follows: $R_{on} = 0.1 \Omega$, $R_L = 1 \text{ k}\Omega$, $C = 10 \mu\text{F}$, $D = 0.5$, $V_{in} = 10 \text{ V}$, Conversion ratio = 4, 6, 10, 16.

As Fig. 4 shows, the PFSCC and Dickson SCC are the SCCs with the highest power efficiencies at the conversion ratio of 4 and 6. At conversion ratio of 10 and 16, the PFSCC has the second highest power efficiencies among others.

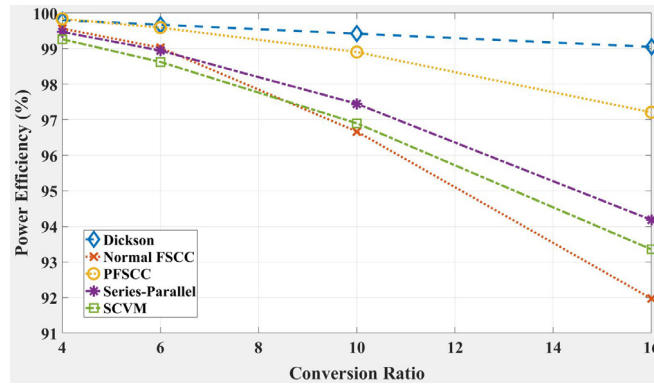


Fig. 4. Power efficiencies at different conversion ratios.

Fig. 5 demonstrates the output ripple voltage at different conversion ratios. The converter with lowest output ripple voltage is the PFSCC. This is because it has the symmetrical structure.

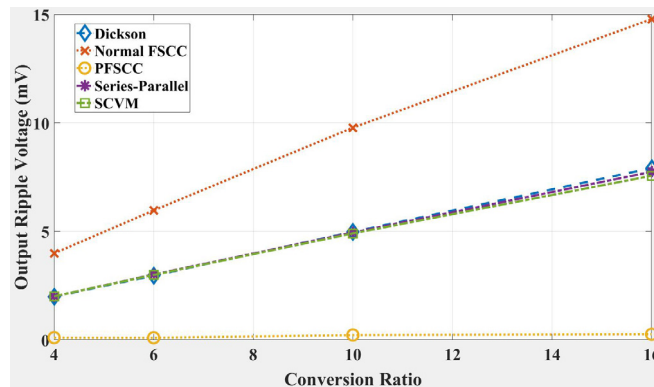


Fig. 5. Output ripple voltage at different conversion ratios.

5. Conclusion

This paper has analyzed the PFSCC. From the analysis, we derive the parameters as follows: output voltage, power efficiency, optimized capacitances of capacitors and power stage transfer function. It is confirmed by the simulations and comparisons that the PFSCC has high power efficiency and low output ripple voltages. If a target system requires an SCC with high power efficiency and low ripple voltage, the PFSCC can be a solution.

For a future study, the obtained parameters will be utilized to design a digital control and a hardware of the PFSCC.

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