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Article

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A step-down nesting-type ac–ac converter combined with voltage equalizers and switched-capacitor simple converters

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Abstract

In this paper, we present an inductor-less direct ac–ac converter with improved nesting-type topology. Unlike existing direct ac–ac converters, the proposed ac–ac converter combines a voltage equalizer and a switched-capacitor (SC) simple converter. Owing to the nesting conversion using two techniques, the proposed converter can provide a stepped-down voltage with small number of circuit components and high input power factor. To evaluate the performance of the proposed ac–ac converter, we compared the proposed ac–ac converter with existing inductor-less ac–ac converters, namely, flying capacitor type converter, symmetrical type converter, and traditional nesting-type converter, by theoretical analysis and simulation program with integrated circuit emphasis (SPICE) simulations. The SPICE simulations demonstrate that the proposed ac–ac converter outperforms existing inductor-less ac–ac converters in the point of circuit size and input power factor, although the power efficiency of the proposed ac–ac converter is inferior to that of the symmetrical type converter. In the case of $1/4\times$ voltage gain, the proposed ac–ac converter achieves about 82% power efficiency and 0.58 input power factor when the output power is 200 W.

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Keywords: Inductor-less ac–ac converter; Nesting-type inverter; Switched-capacitor circuits; Step-down converter; Voltage equalizers

1. Introduction

As an alternative component of auto-transformers, an inductor-less direct ac–ac converter [1,2] has been developed in recent years, where the inductor-less design is realized by the switched-capacitor (SC) technique [3,4]. In the past few years, many challenges have been undertaken to design the inductor-less direct ac–ac converters.

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For example, Lazzarin et al. [2] and Andersen et al. [5] suggested the $1/2 \times 2 \times$ direct ac–ac converter with a flying capacitor. Although the voltage gain of these ac–ac converters is small, these ac–ac converters can provide a simple circuit configuration. Following this study, You and Hui [6] improved the voltage gain of the Lazzarin's flying capacitor type converter to $1/4 \times 4 \times$ by increasing the number of stages. However, due to three flying capacitors, power efficiency and input power factor of these converters are low. To improve the performance of the direct ac–ac converters, Eguchi et al. [7] developed the direct ac–ac converter with symmetrical topology. Since the symmetrical type converter requires no flying capacitor, it can achieve high power efficiency and high input power factor. However, the symmetrical type converter suffers from a large number of circuit components. To overcome this problem, Do et al. [8] and Eguchi et al. [9] proposed the direct ac–ac converter with nesting topology. Unlike the above-mentioned existing converters, the voltage ratio of main capacitors is not constant by utilizing two flying capacitor type converters. Therefore, the nesting-type converter can reduce the number of circuit components. However, there is still room for improvement in the traditional nesting-type converter, because this technique requires two flying capacitors.

In this paper, we present an inductor-less direct ac–ac converter with improved nesting-type topology. Unlike existing direct ac–ac converters, the proposed ac–ac converter combines a voltage equalizer using a flying capacitor and an SC simple converter. Therefore, small size and high input power factor can be achieved by utilizing the nesting conversion. To reveal the characteristics of the proposed converter, theoretical analysis and simulation program with integrated circuit emphasis (SPICE) simulations are conducted. The effectiveness of the proposed ac–ac converter is justified by comparing the proposed converter with the existing converters, namely, flying capacitor type converter [2,5,6], symmetrical type converter [7], and traditional nesting-type converter [8,9].

This reminder of this paper is as follows: First, we explain the circuit configuration of the proposed ac–ac converter in Section 2. Next, theoretical analysis is conducted to clarify the characteristics of the proposed ac–ac converter in Section 3. Then, the effectiveness of the proposed ac–ac converter is justified through performance comparison. Finally, we summarize the result of this work in Section 5.

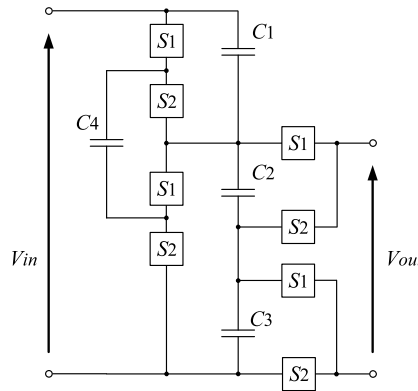


Fig. 1. Circuit configuration of the proposed ac–ac converter.

2. Circuit configuration

The circuit configuration of the proposed ac–ac converter is illustrated in Fig. 1, where S_1 and S_2 are switches driven by two-phase clock pulses. The instantaneous equivalent circuits are shown in Figs. 2(a) and (b). In Figs. 2(a) and (b), R_{on} is the on-resistance of S_i ($i = 1, 2$), $\Delta q_{T_i, v_{in}}$ is the electric charge of V_{in} in State- T_i , and $\Delta q_{T_i, v_{out}}$ is the electric charge of V_{out} in State- T_i .

By combining a voltage equalizer and an SC simple converter, the output voltage is given by

$$V_{out} = \left(\frac{1}{4}\right) \times V_{in}, \quad (1)$$

because the voltage of capacitors satisfies

$$V_{in} = V_{C_1} + V_{C_2} + V_{C_3} \quad \text{and} \quad V_{C_1} = V_{C_2} + V_{C_3} = V_{out} \quad \text{and} \quad V_{C_2} = V_{C_3} \quad (2)$$

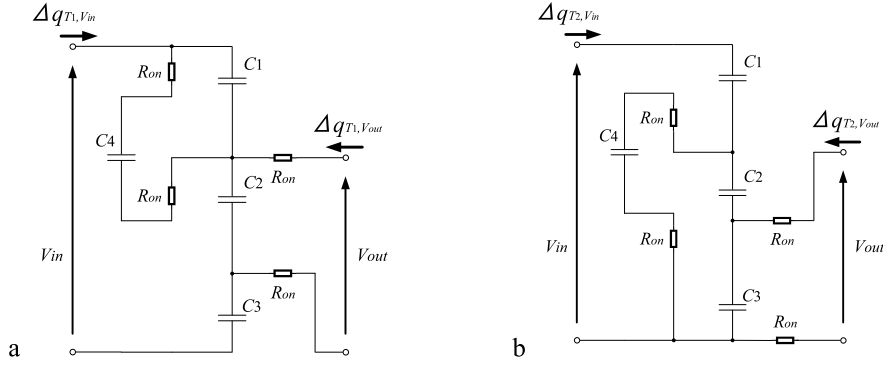


Fig. 2. Instantaneous equivalent circuits: (a) state- T_1 ; (b) state- T_2 .

at a steady state. As Eqs. (1) and (2) show, the proposed converter offers the stepped-down voltage by utilizing nesting conversion. Concretely, by using the flying capacitor C_4 , the voltage of C_1 becomes equal to the voltage of the series-connected capacitors $C_2 + C_3$. Thus, the voltage of C_1 and $C_2 + C_3$ becomes a half of V_{in} . Furthermore, the capacitor C_2 or C_3 is connected to the output terminal, alternately. Therefore, we can obtain a quarter of V_{in} as an output voltage. The detailed theoretical analysis will be given in this next section.

3. Theoretical analysis

To analyze the characteristics of the proposed ac–ac converter, we derive the four-terminal equivalent circuit [10] shown Fig. 3 theoretically. In Fig. 3, m is the turn ratio of an ideal transformer, R_{SC} is the internal resistance of the power converter, and R_L is the output load. To simplify the theoretical analysis, we assumed that 1. Parasitic elements are small and 2. Time constant is much larger the period of clock pulses.

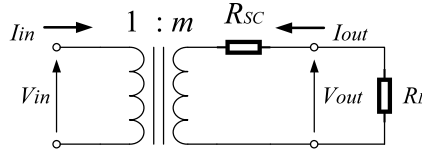


Fig. 3. Four-terminal equivalent model.

First, the relation between the input and the output is obtained by using the instantaneous equivalent circuits shown in Figs. 2(a) and (b). At a steady state, the overall change in electric charges of C_k ($k = 1, \dots, 4$) is zero. Therefore, the differential value of electric charges, $\Delta q_{T_i}^k$, satisfies

$$\Delta q_{T_1}^k + \Delta q_{T_2}^k = 0, \quad (3)$$

where the period of the clock pulse, T , satisfies $T = T_1 + T_2$ and $T_1 = T_2 = T/2$. By using Kirchhoff's current law, the relation between $\Delta q_{T_i}^k$'s is expressed as

$$\Delta q_{T_1, v_{in}} = \Delta q_{T_1}^3 = \Delta q_{T_1}^1 + \Delta q_{T_1}^4, \quad \text{and} \quad \Delta q_{T_2, v_{in}} = \Delta q_{T_2}^1, \quad (4)$$

$$\Delta q_{T_1, v_{out}} = \Delta q_{T_1}^2 - \Delta q_{T_1}^3 = -\Delta q_{T_1}^1 + \Delta q_{T_1}^2 - \Delta q_{T_1}^4, \quad \text{and} \quad \Delta q_{T_2, v_{out}} = -\Delta q_{T_2}^2 + \Delta q_{T_2}^3, \quad (5)$$

$$\Delta q_{T_2}^1 = \Delta q_{T_2}^2 + \Delta q_{T_2}^4, \quad (6)$$

Since the overall change in the electric charges, $\Delta q_{T_i, v_{in}}$ and $\Delta q_{T_i, v_{out}}$, is zero at the steady state, we have the average input/output currents, I_{in} and I_{out} , from Eqs. (3)–(6):

$$I_{in} = \frac{\Delta q_{v_{in}}}{T} = \frac{\Delta q_{T_1, v_{in}} + \Delta q_{T_2, v_{in}}}{T} \quad \text{and} \quad I_{out} = \frac{\Delta q_{v_{out}}}{T} = \frac{\Delta q_{T_1, v_{out}} + \Delta q_{T_2, v_{out}}}{T}. \quad (7)$$

By using Eqs. (3)–(6), Eq. (7) can be rewritten as

$$I_{in} = -\frac{1}{4}I_{out} \quad \text{and} \quad m = \frac{1}{4}. \quad (8)$$

On the other hand, R_{SC} can be obtained from the total consumed energy W_T of Fig. 1. From Figs. 2(a) and (b), the consumed energy W_{Ti} in State- T_i can be given by

$$W_T = W_{T1} + W_{T2} = \left(\frac{5R_{on}}{2}\right) \frac{(\Delta q_{V_{out}})^2}{T}, \quad (9)$$

where

$$W_{T1} = 2R_{on} \frac{(\Delta q_{T1}^4)^2}{T_1} + 2R_{on} \frac{(\Delta q_{T1, V_{out}})^2}{T_1} \quad \text{and} \quad W_{T2} = 2R_{on} \frac{(\Delta q_{T2}^4)^2}{T_2} + 2R_{on} \frac{(\Delta q_{T2, V_{out}})^2}{T_2}. \quad (10)$$

Therefore, we have R_{SC} as $(5/2)R_{on}$, because W_T of Fig. 3 can be expressed as

$$W_T \triangleq \left(\frac{q_{v_{out}}}{T}\right)^2 R_{SC} T. \quad (11)$$

Finally, the four-terminal equivalent circuit can be expressed as the following K-matrix [11]:

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 4 & 0 \\ 0 & \frac{1}{4} \end{bmatrix} \begin{bmatrix} 1 & (5/2)R_{on} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{out} \\ -I_{out} \end{bmatrix}. \quad (12)$$

From Eq. (12), we get the output voltage and the power efficiency as

$$V_{out} = \left(\frac{V_{in}}{4}\right) \times \left\{ \frac{R_L}{R_L + (5/2)R_{on}} \right\} \quad \text{and} \quad \eta = \frac{R_L}{R_L + (5/2)R_{on}}. \quad (13)$$

As Eq. (13) shows, the output voltage becomes $V_{in}/4$ if the internal resistance R_{SC} ($= (5/2)R_{on}$) is negligibly small. Therefore, the proposed ac–ac converter can offer $1/4 \times$ voltage gain.

4. Performance evaluation

In this section, the effectiveness of the proposed ac–ac converter is justified by comparing the proposed ac–ac converter with existing converters, namely, flying capacitor type converter, symmetrical type converter, and traditional nesting-type converter. To evaluate the performance of these converters, we conducted SPICE simulations under the conditions that $V_{in} = 220\text{V}@50\text{ Hz}$, $R_{on} = 0.83\ \Omega$, $f = 100\text{ kHz}$, $C_1 = \dots = C_3 = 33\ \mu\text{F}$, and $C_4 = 3.3\ \mu\text{F}$.

Fig. 4 depicts the simulated output voltage, where R_L was set to $1\text{ k}\Omega$. As Fig. 4 shows, the proposed converter can achieve the $1/4 \times$ voltage gain. Fig. 5 demonstrates the comparison result of power efficiency between the proposed converter and existing converters, namely, flying capacitor type converter [2,5,6], symmetrical type converter [7], and traditional nesting-type converter [8,9]. As you can see from Fig. 5, the power efficiency of the proposed converter is the second highest. When the output power is 200 W , the proposed converter can achieve about 82% power efficiency. Fig. 6 shows the comparison result of input power factor. The input power factor of the proposed converter is the highest when the output power is less than 200 W . About 0.58 input power factor can be achieved by the proposed converter when the output power is 200 W . Table 1 demonstrates the number of circuit components. As Table 1 shows, the number of circuit components of the proposed converter is the smallest among them. Although the performance of the symmetrical type converter is higher than that of the proposed converter, the number of circuit components of the proposed converter is only 60% of that of the symmetrical type converter. Therefore, the proposed topology can offer low cost realization and a simple circuit configuration.

5. Conclusion

To provide the $1/4 \times$ stepped-down voltage, an inductor-less direct ac–ac converter has been proposed in this paper. By combining a voltage equalizer and an SC simple converter, the proposed converter realizes nesting conversion to provide the $1/4 \times$ voltage gain. Concerning existing converters, namely, flying capacitor type converter, symmetrical type converter, and traditional nesting-type converter, the performance analysis was demonstrated by

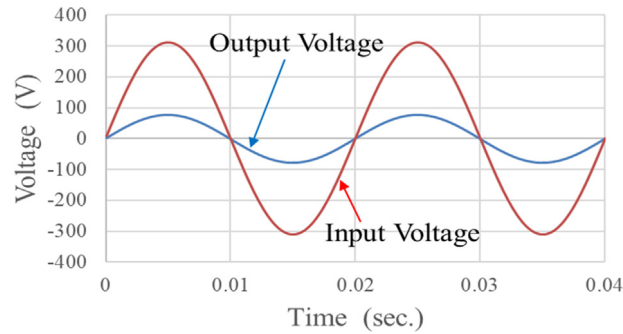


Fig. 4. Simulated output voltage.

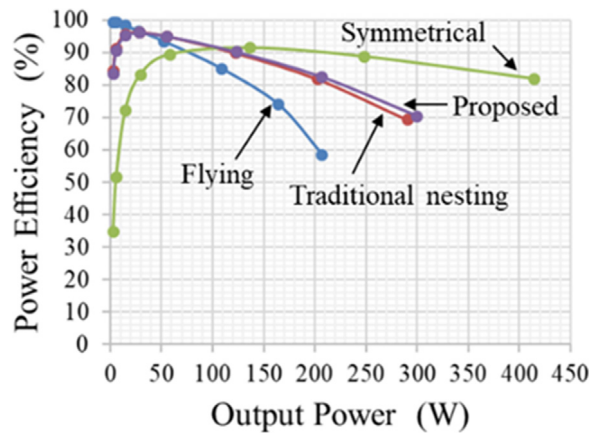


Fig. 5. Simulated power efficiency.

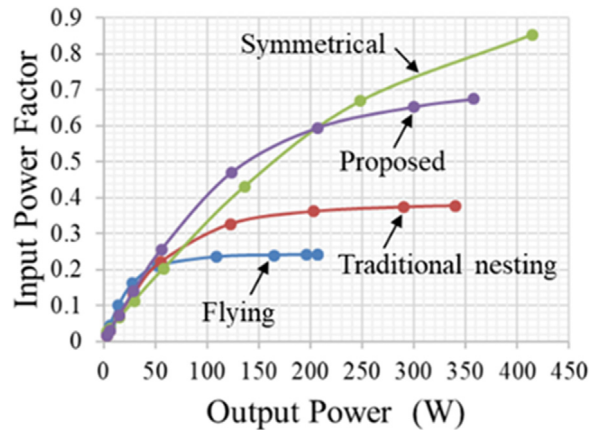


Fig. 6. Simulated input power factor.

theoretical analysis and SPICE simulations. The SPICE simulated results showed the following results: 1. The proposed ac–ac converter achieves about 82% power efficiency and 0.58 input power factor when the output power is 200 W. 2. Although the power efficiency of the proposed converter is the 2nd highest, the number of the circuit components for the proposed converter is smaller than that for the existing converters. Concretely, the number of circuit components of the proposed converter is only 60% of that of the symmetrical type converter.

Table 1. Number of circuit components.

Topology	Gain	Number of switches	Number of capacitors	Total number of circuit components
Proposed ac–ac converter	$1/4\times$	8	4	12
Flying capacitor type	$1/4\times$	8	7	15
Symmetrical type	$1/4\times$	16	4	20
Traditional nesting-type	$1/4\times$	8	5	13

In a future study, we assemble the experimental circuit of the proposed ac–ac converter on a PCB (printed circuit board) and investigate the characteristics of the proposed ac–ac converter experimentally.

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