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Article

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Synthesis and analysis of a cross-connected Fibonacci dc/dc converter with high voltage gain

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Abstract

For thermal energy harvester based on a step-up dc/dc converter, we present a cross-connected Fibonacci dc/dc converter and its analysis method in this paper. The topology of the proposed converter has three features: cross-connection of two Fibonacci-type converters, symmetrical design without smoothing capacitors, and inductor-less design by using switched-capacitor (SC) techniques. From these features, high stepped-up voltage which is expressed as a power of two is provided by the proposed converter. Unlike existing converters, the proposed converter achieves small internal resistance as well as small ripple factor, because the output voltage is supplied to an output load in all clock phases. Furthermore, the inductor-less design offers low electromagnetic interference (EMI) noise, small size, and light weight. As an example of the proposed converter, the performance of the proposed converter with $8\times$ voltage gain was evaluated by theoretical analysis, SPICE simulations, and breadboard experiments. Compared with existing dc/dc converters, namely, Fibonacci type converter, series-parallel type, and charge pump, the proposed converter demonstrated high performance in the point of voltage gain, circuit size, power efficiency, and response speed.

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Keywords: Fibonacci converter; Inductor-less converters; DC/DC converters; Cross-connected structure; Symmetrical structure; High voltage gain

1. Introduction

Energy harvesting techniques provide the potential for infinite clean power. In the energy harvesting system, unconventional energy, such as thermoelectric, light, vibration, is collected by energy harvesters. However, in the thermal energy harvesting, power density of the energy harvesters is very low, and the collected voltage level is insufficient to drive electric devices directly. For this reason, it is necessary to design efficient power converters with high power efficiency as well as high voltage gain.

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In these last few decades, many attempts have been undertaken to design efficient dc/dc converters [1] for thermal energy harvesting. Among others, an inductor-less step-up converter is receiving many researchers’ attention, because it can achieve small size, light weight, and small EMI. For example, an inductor-less dc/dc converter using Fibonacci converter [2,3] was designed to achieve high voltage gain. However, the ripple factor of the Fibonacci-type converter is large. Of course, the ripple factor can be reduced by using a big smoothing capacitor or a parallel topology. However, these techniques require a large occupational layout area. Apart from that, series–parallel converters [4] and a family of charge pumps [5–7] were developed to offer inductor-less design. However, the voltage gains of these dc/dc converters, which is expressed as $N \times$ ($=1, 2, 3, \dots$), is small. Although voltage gain increases in proportion to the number of converter blocks, the circuit size of these converters becomes large.

In this paper, we propose a cross-connected Fibonacci dc/dc converter and its analysis method for thermal energy harvester based on a step-up dc/dc converter. Unlike existing converters, the topology of the proposed converter has three features: cross-connection of two Fibonacci-type converters, symmetrical design without smoothing capacitors, and inductor-less design by using SC techniques. Therefore, the proposed converter can offer high voltage gain, namely, $2^M \times$ ($M = 1, 2, 3, \dots$), small internal resistance, and small ripple noise without big smoothing capacitors. By comparing the proposed converter with the existing converters, namely, Fibonacci type converter [2,3], series–parallel type [4], and charge pump [5–7], the performance of the proposed converter is revealed through theoretical analysis, SPICE simulations, and breadboard experiments.

2. Circuit configuration

Fig. 1 illustrates the circuit configuration of the proposed converter. As Fig. 1 shows, the proposed converter consists of two Fibonacci type converters with cross-connection. The proposed converter by driving S_1 and S_2 by two-phase clock pulses, Φ_1 and Φ_2 . Unlike existing converters, the proposed cross-connected converter generates an output voltage in all clock phases. Therefore, small ripple noise and small internal resistance are achieved without big smoothing capacitors. The output voltage of the proposed converter is given by

$$V_{out} = 2^M \times V_{in}, \quad (M \geq 2) \tag{1}$$

where V_{in} is an input voltage and M is the number of converter blocks. Of course, by increasing the parameter M , the voltage gain of the proposed converter increases exponentially. Since the voltage gain of the traditional Fibonacci converter is expressed as $\{1, 2, 3, 5, 8, 13, \dots\}$, the proposed converter can achieve higher voltage gain than the traditional Fibonacci converter.

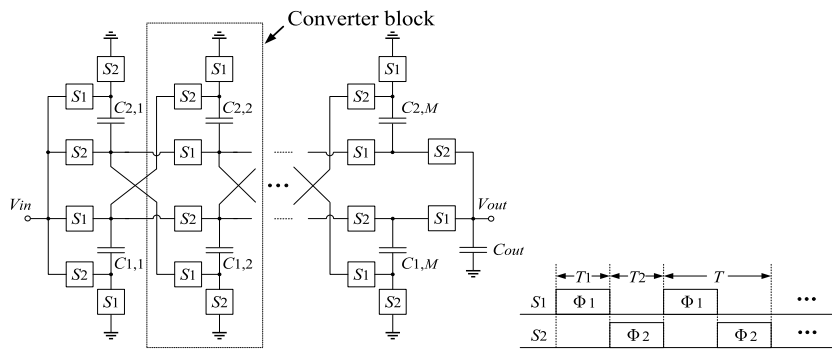


Fig. 1. Circuit configuration of the proposed dual-input cross-connected charge pump with $6 \times$ step-up gain.

3. Theoretical analysis

The general form of the proposed converter is analysed theoretically by utilizing the four-terminal equivalent model [8,9] shown in Fig. 2, where m is the turn ratio of an ideal transformer, R_{SC} is the internal resistance of the power converter, and R_L is the output load. The equivalent circuit of the proposed converter is derived by using the instantaneous equivalent circuits shown in Fig. 3, where R_{on} is the on-resistance of S_i ($i = 1, 2$), $\Delta q_{T_i, v_{in}}$ is the electric charge of V_{in} in State- T_i , and $\Delta q_{T_i, v_{out}}$ is the electric charge of the output terminal in State- T_i . To simplify

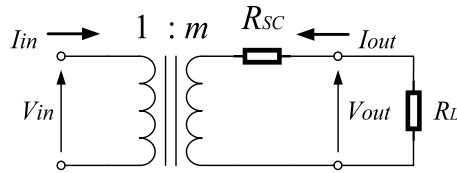
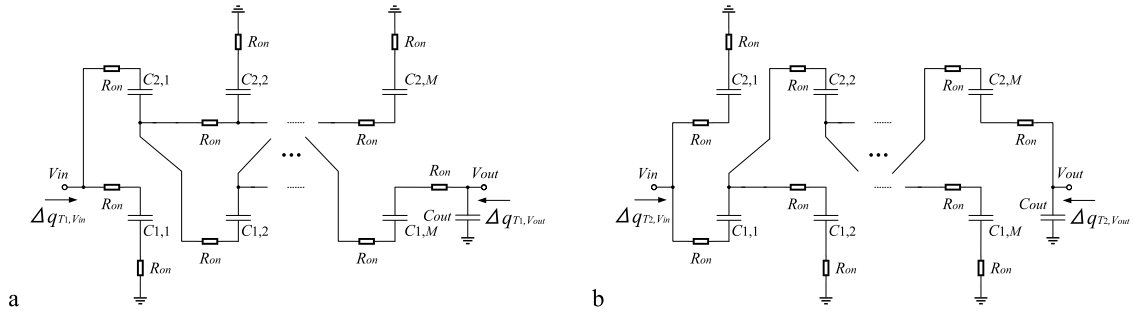


Fig. 2. Four-terminal equivalent model.

Fig. 3. Instantaneous equivalent circuits of the first converter block: (a) state- T_1 ; (b) state- T_2 .

the theoretical analysis, we assume the following conditions: 1. Parasitic elements are small and 2. Time constant is much larger than the period of clock pulses, T .

In a steady state, the differential value of electric charges $\Delta q_{T_i}^{i,j}$ in $C_{i,j}$ ($i = 1, 2$) and ($j = 1, \dots, M$) satisfies

$$\Delta q_{T_1}^{i,j} + \Delta q_{T_2}^{i,j} = 0, \quad (2)$$

Because the overall change in electric charges is zero in the cycle T . In Eq. (2), the interval of T_1 and T_2 satisfies $T = T_1 + T_2$ and $T_1 = T_2 = T/2$. In Fig. 3(a), $\Delta q_{T_1}^{i,j}$ satisfies the following equations by using Kirchhoff's current law:

$$\Delta q_{T_1, v_{in}} = \Delta q_{T_1}^{1,1} - \Delta q_{T_1}^{2,1}, \quad \Delta q_{T_1, v_{out}} = \Delta q_{T_1}^{out} + \Delta q_{T_1}^{1,M}, \quad (3)$$

$$\Delta q_{T_1}^{1,2} = \Delta q_{T_1}^{2,1} + \Delta q_{T_1}^{2,2}, \quad \Delta q_{T_1}^{2,3} = \Delta q_{T_1}^{1,2} + \Delta q_{T_1}^{1,3},$$

$$\Delta q_{T_1}^{1,4} = \Delta q_{T_1}^{2,3} + \Delta q_{T_1}^{2,4}, \quad \Delta q_{T_1}^{2,5} = \Delta q_{T_1}^{1,4} + \Delta q_{T_1}^{1,5},$$

...

$$\Delta q_{T_1}^{1,M} = \Delta q_{T_1}^{2,M-1} + \Delta q_{T_1}^{2,M}. \quad (4)$$

On the other hand, we have the following equations in Fig. 3(b):

$$\Delta q_{T_2, v_{in}} = \Delta q_{T_2}^{2,1} - \Delta q_{T_2}^{1,1}, \quad \Delta q_{T_2, v_{out}} = \Delta q_{T_2}^{out} + \Delta q_{T_2}^{2,M}, \quad (5)$$

$$\Delta q_{T_2}^{2,2} = \Delta q_{T_2}^{1,1} + \Delta q_{T_2}^{1,2}, \quad \Delta q_{T_2}^{1,3} = \Delta q_{T_2}^{2,2} + \Delta q_{T_2}^{2,3},$$

$$\Delta q_{T_2}^{2,4} = \Delta q_{T_2}^{1,3} + \Delta q_{T_2}^{1,4}, \quad \Delta q_{T_2}^{1,5} = \Delta q_{T_2}^{2,4} + \Delta q_{T_2}^{2,5},$$

...

$$\Delta q_{T_2}^{2,M} = \Delta q_{T_2}^{1,M-1} + \Delta q_{T_2}^{1,M}. \quad (6)$$

From Eqs. (2)–(6) and symmetric property of the proposed converter, $\Delta q_{T_i}^{i,j}$ is expressed as

$$\Delta q_{T_1}^{2,2} = -\Delta q_{T_1}^{1,1},$$

$$\Delta q_{T_1}^{1,2} = -\frac{1}{2}\Delta q_{T_1}^{1,1} \quad \text{and} \quad \Delta q_{T_1}^{2,2} = \frac{1}{2}\Delta q_{T_1}^{1,1},$$

$$\Delta q_{T_1}^{1,3} = \frac{1}{4}\Delta q_{T_1}^{1,1} \quad \text{and} \quad \Delta q_{T_1}^{2,3} = -\frac{1}{4}\Delta q_{T_1}^{1,1},$$

$$\Delta q_{T_1}^{1,4} = -\frac{1}{8}\Delta q_{T_1}^{1,1} \quad \text{and} \quad \Delta q_{T_1}^{2,4} = \frac{1}{8}\Delta q_{T_1}^{1,1},$$

...

$$\Delta q_{T_1}^{1,M} = -\frac{1}{2^{M-1}}\Delta q_{T_1}^{1,1}, \quad \text{and} \quad \Delta q_{T_1}^{2,M} = \frac{1}{2^{M-1}}\Delta q_{T_1}^{1,1}, \tag{7}$$

Since the average input/output currents, I_{in} and I_{out} , are expressed as

$$I_{in} = \frac{\Delta q_{v_{in}}}{T} = \frac{\Delta q_{T_1,v_{in}} + \Delta q_{T_2,v_{in}}}{T} \quad \text{and} \quad I_{out} = \frac{\Delta q_{v_{out}}}{T} = \frac{\Delta q_{T_1,v_{out}} + \Delta q_{T_2,v_{out}}}{T}, \tag{8}$$

We get the relation of I_{in} and I_{out} by substituting Eqs. (2)–(7) into Eq. (8):

$$I_{in} = -2^M I_{out} \quad (m = 2^M), \quad \Delta q_{v_{in}} = 4\Delta q_{T_1}^{1,1}, \quad \text{and} \quad \Delta q_{v_{out}} = -\frac{1}{2^{M-2}}\Delta q_{T_1}^{1,1}. \tag{9}$$

Next, in order to obtain R_{SC} , we analyse the total consumed energy, W_T , of Fig. 3. Since the proposed converter has a symmetrical topology, the consumed energy of Fig. 3(a) is equal to that of Fig. 3(b). Therefore, we obtain W_T as

$$\begin{aligned} W_T &= W_{T1} + W_{T2} = 2W_{T1}, \\ &= 2 \times \left\{ 2R_{on} \frac{(\Delta q_{T_1}^{1,1})^2}{T_1} + R_{on} \frac{(\Delta q_{T_1}^{2,1})^2}{T_1} + \dots + 2R_{on} \frac{(\Delta q_{T_1}^{1,M-1})^2}{T_1} + R_{on} \frac{(\Delta q_{T_1}^{2,M-1})^2}{T_1} \right. \\ &\quad \left. + R_{on} \frac{(\Delta q_{T_1}^{1,2})^2}{T_1} + 2R_{on} \frac{(\Delta q_{T_1}^{2,2})^2}{T_1} + \dots + R_{on} \frac{(\Delta q_{T_1}^{1,M})^2}{T_1} + 2R_{on} \frac{(\Delta q_{T_1}^{2,M})^2}{T_1} + R_{on} \frac{(\Delta q_{T_1}^{1,M})^2}{T_1} \right\} \\ &= \left\{ 2^{2(M-1)} \times 3R_{on} \left(\sum_{k=1}^{M-1} \frac{1}{2^{2k}} + 1 \right) + R_{on} \right\} \frac{(\Delta q_{v_{out}})^2}{T}, \end{aligned} \tag{10}$$

where W_{T1} and W_{T2} is the consumed energy in State- T_1 and State- T_2 , respectively. Therefore, R_{SC} is derived as

$$R_{SC} = 2^{2(M-1)} \times 3R_{on} \left(\sum_{k=1}^{M-1} \frac{1}{2^{2k}} + 1 \right) + R_{on}, \tag{11}$$

Because W_T of Fig. 2 can be expressed as

$$W_T \triangleq \left(\frac{q_{v_{out}}}{T} \right)^2 R_{SC} T. \tag{12}$$

Finally, the equivalent circuit of the proposed converter is expressed as

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} \frac{1}{2^M} & 0 \\ 0 & 2^M \end{bmatrix} \begin{bmatrix} 1 & R_{SC} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{out} \\ -I_{out} \end{bmatrix}. \tag{13}$$

From Fig. 2 and Eq. (13), we have the output voltage and the power efficiency as

$$V_{out} = 2^M V_{in} \times \left(\frac{R_L}{R_L + R_{SC}} \right) \quad \text{and} \quad \eta = \frac{R_L}{R_L + R_{SC}}. \tag{14}$$

4. SPICE simulation

Concerning the proposed converter with $8 \times$ step-up gain, SPICE simulations were conducted in order to clarify the characteristics of the proposed converter, where the circuit parameters were set to $V_{in} = 400$ mV, $R_{on} = 1 \Omega$, $f = 1$ MHz, and $C_{1,1} = \dots = C_{2,3} = C_{out} = 500$ pF. The simulated voltage gain is illustrated in Fig. 4, where the proposed converter was compared with the existing converters, namely, Fibonacci type converter [2,3], series-parallel type [4], and charge pump [5–7]. As Fig. 4 shows, the proposed converter can achieve the highest voltage gain with simple circuit control. In proportion to the number of stages, the voltage gain of the proposed converter increases exponentially. As a function of output power, the simulated power efficiency is demonstrated in Fig. 5. In

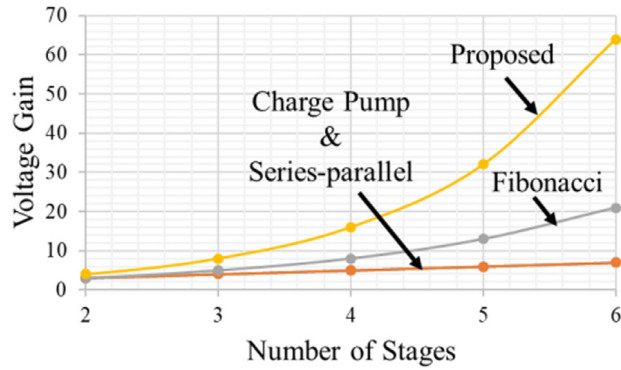


Fig. 4. Simulated voltage gains as a function of the number of stages.

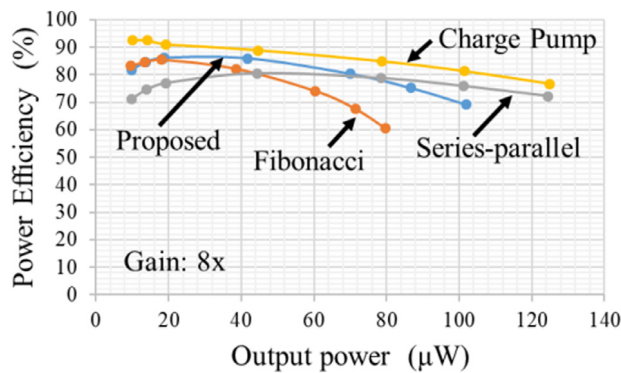


Fig. 5. Simulated power efficiency as a function of output power.

the simulation evaluation for the existing converters, the smoothing capacitor 10nF was connected in parallel with the output load R_L in order to improve power efficiency. As you can see from Fig. 5, the power efficiency of the proposed converter is the second highest among them. This result corresponds to the theoretical results shown in Table 1. The power efficiency of the proposed converter is about 86% when the output power is 40 µW. Fig. 6 shows the transient characteristic when the output load R_L is set to 500 kΩ. As Fig. 6 shows, the proposed converter is the fastest among them, because a big smoothing capacitor is not necessary as shown in Table 1. The proposed converter improves the settling time more than 200 µs from the existing converters.

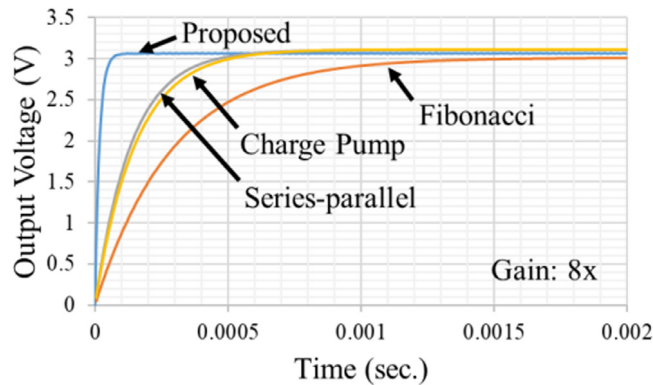


Fig. 6. Simulated transient characteristics.

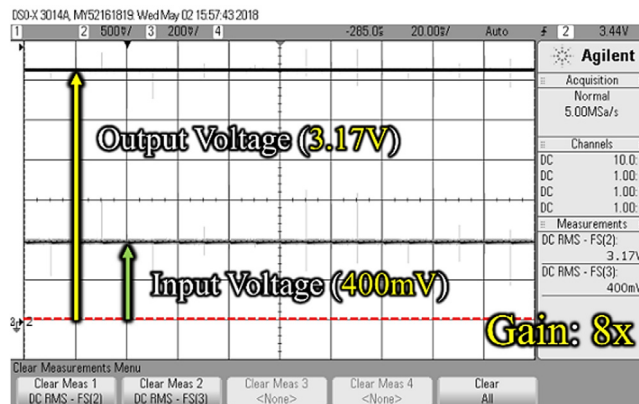
Table 1. Performance comparison between the proposed converter and existing converters with $8\times$ voltage gain.

Topology	Power efficiency	Gain	Number of switches	Number of capacitors	Big smoothing capacitor
Proposed converter	$R_L/(R_L + 64 R_{on})$	$8\times$	20	7	No
Fibonacci type	$R_L/(R_L + 140 R_{on})$	$8\times$	13	5	Yes
Series–parallel type	$R_L/(R_L + 142 R_{on})$	$8\times$	23	8	Yes
Charge pump	$R_L/(R_L + 44 R_{on})$	$8\times$	22	9	Yes

5. Breadboard experiment

Concerning the laboratory prototype of the proposed dc/dc converter, the breadboard experiment was conducted to confirm the feasibility of the converter design, where the experimental circuit was assembled by using commercially available ICs, namely, photo MOS relays AQV 212, darlington sink drivers TD62004APG, a microcontroller PIC, and electrolytic capacitors. Of course, the proposed converter can be integrated into an IC chip, because the proposed topology is an inductor-less design. However, in order to confirm the validity of the proposed topology, we conducted the breadboard experiment. The IC implementation of the proposed converter is left to a future study.

Fig. 7 demonstrates the measured output voltage when V_{in} is about 400 mV and the output load R_L is 510 k Ω . Since the voltage gain of the experimental circuit is $8\times$, the ideal output voltage is 3.2 V. As Fig. 7 shows, the measured output voltage of the laboratory prototype is 3.17 V for the ideal output 3.2 V. From the result of the breadboard experiment, we can confirm the validity of the proposed topology.

**Fig. 7.** Measured output voltage.

6. Conclusion

For thermal energy harvesting applications, this paper has discussed the synthesis and analysis of a cross-connected Fibonacci dc/dc converter. Owing to the inductor-less design with symmetrical topology, the proposed dc/dc converter can provide high voltage gain, small ripple factor, and small internal resistance. Through theoretical analysis, SPICE simulations, and breadboard experiments, the performance of the proposed converter is revealed that 1. The voltage gain of the proposed converter was the highest among that of the existing converters, namely, Fibonacci type converter, series–parallel type converter, and charge pump, because the proposed converter has cross-connected topology; 2. The settling time was improved more than 200 μ s by the proposed technique. Furthermore, the ripple factor of the proposed converter was the smallest among that of existing converters, because a big smoothing capacitor is not needed owing to symmetrical structure; 3. About 86% power efficiency was achieved at 40 μ W output power, because the theoretical analysis demonstrated that the internal resistance of the proposed converter was smallest among the existing converters; and 4. The feasibility of the proposed converter was confirmed by breadboard experiments, where the measured output voltage of the laboratory prototype was 3.17 V for the ideal output 3.2 V.

The proposed inductor-less dc/dc converter can achieve high voltage gain. Thus, the proposed converter will be available to develop an energy harvesting application, such as thermal energy watch.

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