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Article

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A direct high step-down DC/DC converter using cascade ring-type converters

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Abstract

For data center applications, we present a direct high step-down DC/DC converter designed by using switched capacitor (SC) techniques. To achieve high step-down conversion, the proposed converter connects a novel cascade ring-type converter to a traditional buck converter. Unlike existing high step-down SC DC/DC converters, such as ladder-type SC converter, the proposed cascade ring-type converter provides $(1/4)^2 \times$ stepped-down voltage by using four-phase clock pulses, where a 48 V input is converted to 3 V. In the buck converter, the output of the cascade ring-type converter is converted to $3D$ V ($0 < D < 1$). Hence, the proposed converter can achieve the $(D/16) \times$ voltage gain by converting the 48 V input twice. Furthermore, small size and light weight are offered by the proposed converter with a single inductor. The performance of the proposed converter is evaluated by theoretical analysis, computer simulations, and bread board experiments. The evaluation results demonstrate that the proposed converter outperforms the conventional ladder-type SC converter in the point of power efficiency and output voltage.

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Keywords: DC/DC converters; Step-down converters; Cascade connections; Ring-type converters; Data center applications

1. Introduction

For 48 V data center architecture, a high step-down dc/dc converter is receiving many researchers' attention. To achieve high step-down gain, several attempts have already been undertaken in past studies. For example, Saadatizadeh et al. [1] proposed two new transformerless high step-down dc/dc converters and [2] suggested a high-step-down dc–dc converter using coupled-inductors. However, these converters are bulky, because several inductors are necessary to design these power converters. On the other hand, some researchers developed an inductor-less step-down dc/dc converter, such as exponential step-up/step-down type switched-capacitor (SC) converter proposed

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by [3], Dickson-type adder/subtractor dc/dc converter suggested by Eguchi et al. [4], and step-up/step-down k ($=2, 3, \dots$)-Fibonacci dc–dc converter developed by Eguchi et al. [5]. However, the output regulation of these converters is poor. To overcome these problems, Lazzarin et al. [6] proposed a high step-down converter by combining the buck converter with the Ladder-type SC converter. By using a single inductor and cascade-connection of Ladder-type cells, Lazzarin’s converter achieves not only small size but also flexible output regulation. However, there is still room for improvement in power efficiency.

In this paper, we present a direct high step-down SC dc/dc converter for data center applications. In the proposed converter, a novel cascade ring-type converter and a traditional buck converter are connected in series. Unlike existing high step-down SC dc/dc converters, such as ladder-type SC converter [6], the proposed cascade ring-type converter provides $(1/4)^2 \times$ stepped-down voltage by using four-phase clock pulses, where a 48 V input is converted to 3 V. In the buck converter, the output of the cascade ring-type converter is converted to $3D$ V ($0 < D < 1$). Hence, the proposed converter can achieve the $(D/16) \times$ voltage gain by converting the 48 V input twice. Furthermore, small size and light weight are offered by the proposed converter with a single inductor. To evaluate the performance of the proposed converter, theoretical analysis, computer simulations, and bread board experiments are conducted.

2. Circuit configuration

The circuit configuration of the proposed high step-down converter is illustrated in Fig. 1. As Fig. 1 shows, the proposed converter is composed of a cascade ring-type converter and a buck converter. By driving the transistor switches, S_1, \dots, S_9 , cyclically by four-phase clock pulses, the proposed high step-down converter generates the following output voltage:

$$V_{out} = (D/16) \times V_{in}, \quad (0 < D < 1) \tag{1}$$

where V_{in} is an input voltage and D is the duty factor of the buck converter. In Eq. (1), the $D \times$ voltage gain is achieved by the buck converter. On the other hand, the $(1/16) \times$ voltage gain is realized by the cascade ring-type converter. By connecting from C_1 to C_4 in series, the voltage of the capacitor C_1, \dots, C_4 becomes $V_{in}/4$ in the 1st block. After that, each voltage of C_1, \dots, C_4 is converted again in the 2nd block. Since the 2nd converter has the same structure as the 1st converter, the voltage of the capacitor C_5, \dots, C_8 becomes $V_{in}/16$. Therefore, the cascade ring-type converter generates $(1/16)V_{in}$.

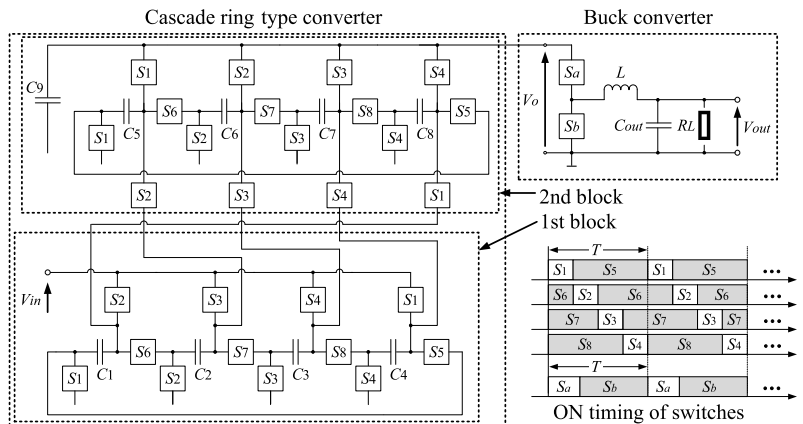


Fig. 1. Proposed high step-down converter.

3. Theoretical analysis

In this section, the characteristics of the proposed converter is analyzed theoretically by using the four-terminal equivalent model [7]. To save space, we discuss the theoretical analysis of the cascade ring-type converter only, because the theoretical analysis of the buck converter is well-known. To simplify the theoretical analysis, the theoretical analysis is conducted under the conditions that 1. On-resistance of all transistor switches S_j ($j = 1,$

..., 8) is R_{on} ; 2. Parasitic elements are negligibly small; and 3. Time constant is much larger than the period of clock pulses, T .

In a steady state, the differential value of electric charges, $\Delta q_{T_i}^k$, in C_k ($(i = 1, \dots, 4)$ and $(k = 1, \dots, 9)$) satisfies

$$\sum_{i=1}^4 \Delta q_{T_i}^k = 0, \tag{2}$$

where $T = \sum_{i=1}^4 T_i$ and $T_1 = T_2 = T_3 = T_4 = T/4$. (3)

Because the overall change in $\Delta q_{T_i}^k$ is zero in the cycle T . Using Kirchoff’s current law, we have the relation between the electric charge of V_{in} in State- T_i , $\Delta q_{T_i, v_{in}}$, and the electric charge of the output terminal V_o in State- T_i , $\Delta q_{T_i, v_o}$ as follows:

$$\Delta q_{T_i, v_{in}} = \Delta q_{T_i}^r, \quad \text{where } r = \begin{cases} i + 3 & \text{if } i = 1 \\ i - 1 & \text{if } i > 1. \end{cases} \tag{4}$$

$$\Delta q_{T_i, v_o} = \Delta q_{T_i}^9 + \Delta q_{T_i}^{i+4} - \Delta q_{T_i}^s, \quad \text{where } s = \begin{cases} i + 5 & \text{if } i \leq 3 \\ i + 1 & \text{if } i = 4. \end{cases} \tag{5}$$

$$\Delta q_{T_i}^a = \Delta q_{T_i}^b = \Delta q_{T_i}^c, \tag{6}$$

where $a = \begin{cases} i + 1 & \text{if } i \leq 3 \\ i - 3 & \text{if } i = 4, \end{cases} \quad b = \begin{cases} i + 2 & \text{if } i \leq 2 \\ i - 2 & \text{if } i > 2, \end{cases} \quad \text{and } c = \begin{cases} i + 3 & \text{if } i = 1 \\ i - 1 & \text{if } i > 1. \end{cases}$

$$\Delta q_{T_i}^{a+4} = \Delta q_{T_i}^{b+4} = \Delta q_{T_i}^{c+4}. \tag{7}$$

$$\Delta q_{T_i}^a = \Delta q_{T_i}^i = \Delta q_{T_i}^{c+4}. \tag{8}$$

Using Eqs. (4) and (5), the average input/output currents, I_{in} and I_{out} , can be expressed as

$$I_{in} = \frac{\Delta q_{v_{in}}}{T} = \frac{1}{T} \sum_{i=1}^4 \Delta q_{T_i, v_{in}} \quad \text{and} \quad I_o = \frac{\Delta q_{v_o}}{T} = \frac{1}{T} \sum_{i=1}^4 \Delta q_{T_i, v_o}. \tag{9}$$

Substituting Eqs. (2)–(8) into Eq. (9), we get the relation of I_{in} and I_{out} as follows:

$$\Delta q_{v_{in}} = -\frac{1}{16} \Delta q_{v_o}, \quad I_{in} = -\frac{1}{16} I_o, \quad \text{and} \quad m_1 = -\frac{1}{16}, \tag{10}$$

because the cascade ring-type converter has a symmetrical structure.

Next, the consumed energy of the cascade ring-type converter is discussed to obtain the internal resistance R_{SC1} . Since the cascade ring-type converter has a symmetrical structure, the total consumed energy W_T can be expressed as

$$\begin{aligned} W_T &= \sum_{i=1}^4 W_{T_i} = 4W_{T_1} \\ &= 4 \times \left\{ R_{on} \frac{(\Delta q_{T_1}^1)^2}{T_1} + 4R_{on} \frac{(\Delta q_{T_1}^2)^2}{T_1} + 4R_{on} \frac{(\Delta q_{T_1}^2 - \Delta q_{T_1}^1)^2}{T_1} + R_{on} \frac{(\Delta q_{T_1}^5)^2}{T_1} \right. \\ &\quad \left. + R_{on} \frac{(\Delta q_{T_1}^5 + \Delta q_{T_1}^1 - \Delta q_{T_1}^2)^2}{T_1} \right\} \\ &= \left(\frac{477}{256} \right) R_{on} \frac{(\Delta q_{V_o})^2}{T}. \end{aligned} \tag{11}$$

From Eq. (11), we have R_{SC1} as $(477/256)R_{on}$, because W_T of Fig. 2 can be expressed as

$$W_T \triangleq R_{SC} \frac{(\Delta q_{V_{out}})^2}{T}. \quad (12)$$

Therefore, the equivalent circuit of the cascade ring-type converter is expressed as

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1/m_1 & 0 \\ 0 & m_1 \end{bmatrix} \begin{bmatrix} 1 & R_{SC1} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_o \\ -I_o \end{bmatrix}. \quad (13)$$

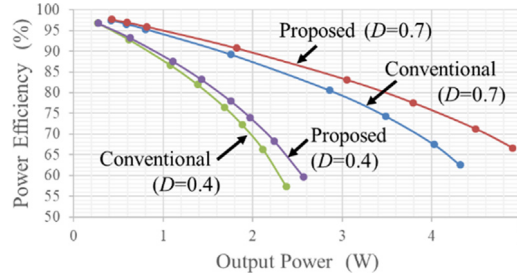


Fig. 2. Simulated power efficiency as a function of output power.

As the reference [6] shows, the conventional high step-down converter is designed by connecting the ladder-type converter and the buck converter in series. Therefore, the total performance of the high step-down converters depends on the performance of the converter blocks, namely, cascade ring-type converter and ladder-type converter. Table 1 shows the performance comparison between the proposed cascade ring-type converter and the conventional ladder-type converter. As Table 1 shows, the power efficiency and output voltage of the proposed cascade ring-type converter is higher than that of the conventional ladder-type converter, because the proposed cascade ring-type converter has small internal resistance R_{SC1} . Therefore, the proposed high step-down converter outperforms the conventional high step-down converter.

Table 1. Performance comparison between the proposed cascade ring-type converter and the conventional ladder-type converter.

Converter name	Gain	R_{SC1}	Power efficiency	Output voltage V_o
Cascade ring-type converter	1/16	$(477/256)R_{on}$	$R_L / \{R_L + (477/256)R_{on}\}$	$V_{in} \times R_L / [16\{R_L + (477/256)R_{on}\}]$
Ladder-type converter [6]	1/16	$(85/32)R_{on}$	$R_L / \{R_L + (85/32)R_{on}\}$	$V_{in} \times R_L / [16\{R_L + (85/32)R_{on}\}]$

4. Simulations

To clarify the effectiveness of the proposed converter, the characteristics of the proposed converter are compared with that of the conventional ladder-type SC converter [6] through simulation program with integrated circuit emphasis (SPICE) simulations. The SPICE simulations were conducted under the conditions that $V_{in} = 48$ V, $R_{on} = 0.1 \Omega$, $C_1 = \dots = C_9 = 33 \mu\text{F}$, $C_{out} = 10 \mu\text{F}$, $L = 10 \mu\text{H}$, and $f = 500$ kHz.

Fig. 2 demonstrates the simulated power efficiency, and Fig. 3 depicts the simulated output voltage. As Fig. 2 shows, the proposed converter can achieve higher power efficiency than the conventional converter. Concretely, the proposed converter can achieve 83% efficiency when $D = 0.7$ and the output power $P_{out} = 3$ W. When $D = 0.4$ and $P_{out} = 2$ W, the proposed converter can achieve 73% efficiency. Furthermore, these simulation results agree well with the theoretical results shown in Table 1. Of course, the output power of the proposed converter can be increased by connecting the proposed converter in parallel. On the other hand, as Fig. 3 shows, the proposed converter has flexibility of voltage gain by controlling the duty factor D . From these simulation results, we can confirm the effectiveness of the proposed converter.

5. Experiments

To confirm the feasibility of the proposed topology, the experimental circuit of the proposed converter was built with commercially available ICs, namely, photo MOS relays AQV 212, darlington sink drivers TD62004APG, a

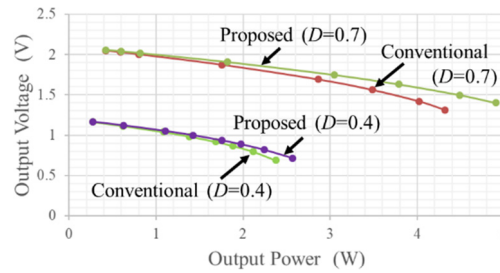


Fig. 3. Simulated output voltage as a function of output power.

microcontroller PIC, and electrolytic capacitors, on a breadboard. Fig. 4 demonstrates the measured output voltage, where the input voltage $V_{in} = 24$ V, $C_1 = \dots = C_9 = 33$ μ F, $C_{out} = 100$ μ F, $L = 100$ mH, $f = 40$ Hz, and the output load $R_L = 100$ k Ω . As Fig. 4 shows, the experimental circuit can achieve high step-down gain. Concretely, the voltage gain is about 1/53 when $D = 0.4$. On the other hand, the voltage gain is about 1/19 when $D = 0.7$. Hence, we can confirm the feasibility of the proposed topology from these experimental results.



Fig. 4. Measured output voltage: (a) $D = 0.4$ V; (b) $D = 0.7$ V.

6. Conclusion

For data center applications, a direct high step-down dc/dc converter using cascade ring-type converters has been proposed in this paper. By comparing the conventional ladder-type SC converter, the effectiveness of the proposed converter was clarified through theoretical analysis, computer simulations, and bread board experiments. The comparison results showed that 1. The proposed converter can achieve higher power efficiency than the conventional converter. Concretely, the proposed converter can achieve 83% efficiency when $D = 0.7$ and $P_{out} = 3$ W. On the other hand, when $D = 0.4$ and $P_{out} = 2$ W, the proposed converter can achieve 73% efficiency. These simulation results agreed well with the theoretical results; and 2. The feasibility of the proposed topology was confirmed by experiments. The experimental circuit achieved high step-down gain, namely, $1/53\times$ and $1/19\times$, from a 24 V input. In a future study, we are going to investigate the characteristics of the proposed converter through experiments.

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