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Article

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Research paper

Enhancement of voltage profile by incorporation of SVC in power system networks by using optimal load flow method in MATLAB/Simulink environments

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ABSTRACT

Flexible AC Transmission Systems (FACTS) controllers could be a suitable alternative to provide reactive power support at the load centers locally and hence keep the voltages within their safe operating limits. Due to high costs of FACTS devices, their proper location in the system must be ascertained. The fundamental object of this thesis work is to improve the voltage profile by reducing the real and reactive power loss in the system. The voltage profile in the system is being improved by using the FACTS device Static VAR Compensator (SVC). In this paper, studies and analyzes SVC technology for voltage enhancement, reducing system losses, suppression of fluctuations. The effectiveness of the proposed method has been tested on IEEE-9 and IEEE-30 bus systems. Optimal placement has been obtained for the base case loading and to verify its locations. To achieve the optimization of the location and the size of the power system to optimize the system performance. A Newton–Raphson Load Flow problem has been formulated with an objective to improve the voltage profile with minimization of the losses. Moreover, the effects of SVC on economic condition have also been investigated. The results obtained are in the form of the plot and compared with the plots without SVC. This work also helpful for those persons are working in the field of FACTS controllers planning.

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1. Introduction

Modern power systems are becoming more vulnerable to operating limit violation and voltage instability problems due to large transmission networks, deregulation of the electricity industry and utilization of various renewable energy sources as well as different load patterns. As power systems have evolved through continuing growth in interconnections, use of new technologies and controls, and the increased operation in highly stressed conditions, different forms of system instability have emerged. For example, voltage stability, frequency stability and interrelated oscillations have become greater concerns than in the past. This has created a need to review the definition and classification of power system stability. Now a day's many methods are used to generate and to control the reactive power without the use of the capacitors and the reactor banks like Gate Turn-off thyristors. Other well advance technologies, Flexible Alternating Current Transmission System (FACTS) (Mithulananthan et al., 2003; Ou and Singh, 2002; Gerbex et al., 2001; Huang and Yan, 2002; Dixon et al., 2005; Singh et al., 2006; Mahdad

et al., 2006; Mondal et al., 2012; Mark Ndubuka, 0000; Minguez et al., 2007; Jannati et al., 2008; Musunuri and Dehnavi, 2010; Kamarposhti and Alinezhad, 2009; Singh et al., 2011; Acha and Kazemtabrizi, 2013; Palukuru and Nee Dey, 2014; Gabbar and Abdelsalam, 2014; Singh et al., 2015; Athamneh and Lee, 2006; Ghorbani et al., 2012; Hingorani and Gyugyi, 2000; Dixon et al., 2005; Khanmohammadi et al., 2007; Venkateswara Rao et al., 2009; Srivastava, 2012; Grudin and Roytelman, 1997; Taylor et al., 2005; Stahlkopf and Wilhelm, 1997; Grünbaum et al., 2003; Kundur, 1994; Taylor, 1994) have been discovered that are used in the transmission system to improve the power quality and to compensate the reactive power (Stahlkopf and Wilhelm, 1997; Grünbaum et al., 2003). FACTS have different devices for the above mentioned functions like Static VAR Compensators (SVC), Unified Power Flow Compensators (UPFC) and the Static Synchronous Compensator (STATCOM) (Kundur, 1994; Taylor, 1994).

1.1. Literature review

Mithulananthan et al. (2003), discussed and compares different control techniques for damping undesirable inter area oscillation in power systems by means of power system stabilizers (PSS), static VAR compensators (SVCs), and shunt static synchronous

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Abbreviations

AVR	Automatic Voltage Regulator
FACTS	Flexible Alternating Current Transmission Systems
TSC	Thyristor Switched Capacitor
OEL	Over Excitation Limiter
DGs	Distributed generations
OPF	Optimal Power Flow
GA	Genetic algorithms
SVC	Static Var Compensator
LFA	Load flow analysis
TCR	Thyristor Controlled Reactor
VP	Residential load models
TCSC	Thyristor Controlled Series Capacitor
NRLF	Newton–Raphson Load Flow
STATCOM	Static-synchronous compensator

Symbols

SVC	Static Var Compensator (p.u.)
α	Real power exponent
β	Reactive power exponent
P_{m_bus}	Real power of static load (p.u.)
P_L	Real power loss of the system (p.u.)
AP, RP	Real and reactive power supported to the system
Q_{intake_sys}	Reactive power intake of system (p.u.)
AP_{SVC}, RP_{SVC}	Real power and reactive power delivered to the system by SVC
f	Supply frequency (50 Hz)
OPF	Operating power factor
Q_{m_bus}	Reactive power of static load (p.u.)
FACTS	Flexible Alternating Current Transmission Systems
P,Q	Real power and reactive power supported to the system
S_{intake_sys}	Apparent power intake of system (p.u.)

compensators (STATCOMs). [Ou and Singh \(2002\)](#), discussed the Total transfer capability (TTC), which is usually limited by overloaded circuits and buses with relatively low voltage. Flexible AC transmission system (FACTS) technology can redistribute load flow and regulate bus voltage, so it is a promising method to improve TTC. [Gerbex et al. \(2001\)](#), presented a genetic algorithm to seek the optimal location of multi-type FACTS devices in a power system. The optimizations are performed on three parameters: the location of the devices, their types and their values. The system load ability is applied as a measure of power system performance. Four different kinds of FACTS controllers are used and modeled for steady-state studies: TCSC, TCPST, TCVR and SVC. Simulations are done on a 118-bus power system for several numbers of devices. Results show the difference of efficiency of the devices used in this context. [Huang and Yan \(2002\)](#), investigated the effect of thyristor controlled series capacitor (TCSC) and static VAR compensator (SVC) on power system load curtailments. An algorithm of optimal power flow (OPF) to reduce the load curtailment for installing TCSC/SVC in the system is proposed in this paper. [Dixon et al. \(2005\)](#), presented an overview of the state of the art in reactive power compensation technologies. The principles of operation, design characteristics and application examples of VAR compensators implemented with thyristors and self-commutated converters are presented. Static VAR generators are used to improve voltage regulation, stability, and power factor in ac transmission and distribution systems. [Singh et al. \(2006\)](#), presented the continuous change in power

demand and supply altered the power flow patterns in transmission networks in such a way that some of the corridors are lightly loaded and some of the corridors get over loaded. To cope with these problems, flexible AC transmission systems (FACTS) are used. This paper suggests a new sensitivity based approach to locate thyristor controlled series compensator (TCSC) and unified power flow controller (UPFC) for enhancing the power system load ability. The effectiveness of the proposed method is tested and illustrated on 5-bus and IEEE 14-bus systems. [Mahdad et al. \(2006\)](#), focused on the first two of these requirements choosing the type of FACTS devices, deciding the installation location and control of FACTS. We presented a simple algorithm based in heuristic and practical rules to seek the optimal location of two types of FACTS, shunt compensation 'SVC' and series compensation 'TCSC'. The system load ability and loss minimization are applied as a measure of power system performance. Results show the impact of optimal operating points of FACTS (SVC and TCSC) devices under various conditions of power system. [Mondal et al. \(2012\)](#), investigated the optimal location and setting parameters of SVC (Static VAR Compensator) and TCSC (Thyristor Controlled Series Compensator) controllers using PSO (Particle Swarm Optimization) to mitigate small signal oscillations in a multi machine power system. Installations of FACTS devices have been suggested in this paper to achieve appreciable damping of system oscillations. However the performance of FACTS devices highly depends upon its parameters and suitable location in the power network. In this paper the PSO based technique is used to investigate this problem in order to improve the small signal stability. [Mark Ndubuka \(0000\)](#), investigated the effects of Static VAR Compensator (SVC) on voltage stability of a power system. The functional structure for SVC built with a Thyristor Controlled Reactor (TCR) and its model are described. The model is based on representing the controller as Variable impedance that changes with the firing angle of the TCR. [Minguez et al. \(2007\)](#), addressed the optimal placement of static VAR compensators (SVCs) in a transmission network in such a manner that its loading margin is maximized. A multi scenario framework that includes contingencies is considered. This problem is formulated as a nonlinear programming problem that includes binary decisions, i.e., variables to decide the actual placement of the SVCs. [Jannati et al. \(2008\)](#), analyzed instability is one of the phenomena which have result in a major blackout. To maintain security of such systems, it is desirable to plan suitable measures to improve power system security and increase voltage stability margins. FACTS devices can regulate the active and reactive power control as well as adaptive to voltage-magnitude control simultaneously because of their flexibility and fast control characteristics. This paper presents a Genetic Algorithm (GA) based allocation algorithm tested on IEEE 30 bus for FACTS devices considering Cost function of FACTS devices and power system losses. [Musunuri and Dehnavi \(2010\)](#), presented a comparison of four Flexible AC Transmission Systems (FACTS) controllers, the Static VAR Compensator (SVC), the Static synchronous Compensator (STATCOM), the Thyristor Controlled Series Compensator (TCSC) and the Static Synchronous Series Compensator (SSSC) on power system steady state voltage stability. [Kamarposhti and Alinezhad \(2009\)](#), presented that the growing concerns over environmental impacts, conditions for improvement of the whole distribution network, and rebate programs offered by governments have contributed to an increment in the number of DG units in commercial and domestic electrical power output. This paper introduces a sensitivity analysis to determine the optimal sitting and sizing of DG units. A new methodology PSO for the placement of DG in the radial distribution systems reduced the active power losses and to improve the voltage profile. The effectiveness of the proposed method is demonstrated through IEEE 16 bus standard test systems. [Singh et al. \(2011\)](#), presented the introduction of Various FACTS controllers such as SVC, TCSC, TCPAR

or TCPAT, SSSC, STATCOM, UPFC, IPFC, GUPFC, HPFC for operation, control, planning & protection from different performance point of view such as increased the load ability, improve the voltage profile, minimize the active power losses, increased the available transfer capacity, enhance the transient and steady-state stability, and flexible operations of power systems. Acha and Kazemtabrizi (2013), presented a new model of the STATCOM aimed at power flow solutions using the Newton–Raphson method. The STATCOM is made up of the series connection of a voltage-source converter (VSC) and its connecting transformer. The VSC is represented in this paper by a complex tap-changing transformer whose primary and secondary windings correspond, notionally speaking, to the VSC's ac and dc buses, respectively. Palukuru and Nee Dey (2014), analyzed instability is considered as a main threat to stability, security, and reliability in the modern power systems. This paper presents a novel method to assess voltage stability status using a unique two-bus π -network equivalent derived with OPF solution of the actual system at different operating conditions. This paper considers an SVC and a TCSC in OPF formulation to assess voltage stable states of any interconnected power system in terms of its reduced two-bus integrated π -equivalent system. Gabbar and Abdelsalam (2014), discussed a high performance dynamic model of a micro-grid system comprising a wind turbine, a PV, a fuel cell, a micro gas turbine generator, an energy storage, electric loads with Variable load profile and flexible AC transmission system (FACTS) devices. The FACTS devices based on static VAR compensators have been employed as a supervisory controller. Singh et al. (2015), presented a comprehensive survey on application of Various conventional, optimization and artificial intelligence (AI) based computational techniques for impact assessment of optimally placed and coordinated control of distributed generations (DGs) and flexible AC transmission systems (FACTS) controllers in power systems (PSs). Athamneh and Lee (2006), studied the impact of FACTS on the performance of Jordanian transmission system under different levels of power exchange with Egyptian and Syrian power systems. This helps to determine the appropriate types and locations for FACTS devices to be installed to improve these limits. Ghorbani et al. (2012), investigated the impact of Static VAR Compensator (SVC) on the apparent impedance seen by the transmission line distance relay. It is shown that the connection type of the windings of the shunt coupling transformer of the SVC has a remarkable effect on the apparent impedance seen by the distance relay.

1.2. Contribution of paper

In this paper, FACTS controller such as SVC is incorporated in the power system network for the improvement of voltage profile and minimization of system loss and cost of the system by using NRLF method. The graphical comparisons of results are also presented in this paper. The effectiveness of the proposed method has been tested on IEEE-9 and IEEE-30 bus systems.

1.3. Organization of paper

The organization of paper are as follows: Section 1 discusses the introduction of power system stability. Section 2 describes the mathematical problem formulation, introduction of various FACTS controller, basic structure and components of SVC, mathematical model of SVC. Section 3 discusses the simulation results deals with the voltage profile of IEEE-9 bus test system and IEEE-30 bus test system with and without SVC using Newton–Raphson load flow method technique.

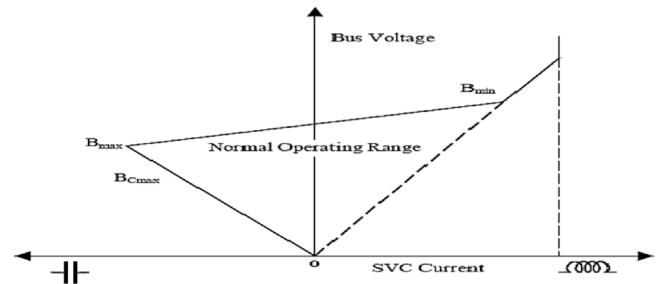


Fig. 2.1. V–I characteristic of SVC.

2. Mathematical problem formulation

The objective function of the optimal placement of SVC includes improvement in voltage profile, reduction of the total real and reactive power loss of the system and overall cost of the system. The most common constraints are considered in this analysis such as power flow equality constraints, bus voltage or voltage drop limits and transmission line overloading capacity for the optimal placement SVC in power systems.

2.1. Different types of FACTS controller

In general FACTS controllers can be divided into four categories:

- Series controllers:* Static Synchronous Series Compensator (SSSC) and Thyristor Controlled Series Capacitor (TCSC) are examples of series FACTS controllers.
- Shunt controllers:* Static VAR Compensator (SVC) and Synchronous Compensator (STATCOM) are examples of shunt FACTS controllers.
- Combined series–series controllers:* Interline power flow controller (IPFC), Thyristor-Controlled Voltage Limiter (TCVL) and Thyristor-Controlled Voltage Regulator (TCVR) are examples of series–series FACTS controllers.
- Combined shunt–series controllers:* Thyristor Controlled Phase Shifting Transformer (TCPST) and Unified Power Flow Controller (UPFC) are examples of shunt–series FACTS controllers.

2.2. V–I characteristics of SVC

The SVC can be operated in two different modes: voltage regulating mode and VAR control mode. When the SVC is operated in voltage regulation mode, it implements following V–I characteristic shown in Fig. 2.1.

2.3. Mathematical modeling of SVC

The SVC firing angle model is implemented in this paper. Thus, the model can be developed with respect to a sinusoidal voltage, differential and algebraic equations are as follows:

$$I_{SVC} = -jB_{SVC}V_k$$

The fundamental frequency TCR equivalent reactance X_{TCR} is given by:

$$X_{TCR} = \frac{\pi XL}{\sigma - \sin\sigma}$$

where $\sigma = 2(\pi - \alpha)$, $X_L = \omega L$

Table 3.1
Parameter for 9 buses test system.

Bus_i	Type	P_d	Q_d	G_s	B_s	Area	V_m	V_a	Base kV	Zone	V_{max}	V_{min}
1	3	0	0	0	0	1	1	0	345	1	1.1	0.9
2	2	0	0	0	0	1	1	0	345	1	1.1	0.9
3	2	0	0	0	0	1	1	0	345	1	1.1	0.9
4	1	0	0	0	0	1	1	0	345	1	1.1	0.9
5	1	90	30	0	0	1	1	0	345	1	1.1	0.9
6	1	0	0	0	0	1	1	0	345	1	1.1	0.9
7	1	100	35	0	0	1	1	0	345	1	1.1	0.9
8	1	0	0	0	0	1	1	0	345	1	1.1	0.9
9	1	125	50	0	0	1	1	0	345	1	1.1	0.9

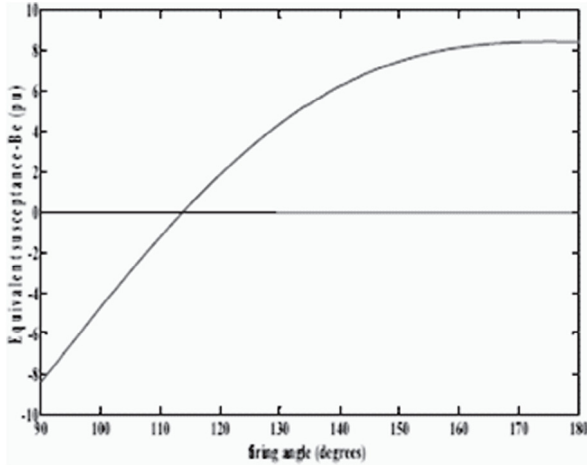


Fig. 2.2. SVC equivalent susceptance profile.

And in terms of firing angle,

$$X_{TCR} = \frac{\pi XL}{[2(\pi - \alpha) + \sin 2\alpha]}$$

where σ and α is conduction and firing angle respectively.

At $\alpha = 90^\circ$, TCR conducts fully and the equivalent reactance X_{TCR} becomes X_L while at $\alpha = 180^\circ$, TCR is blocked and its equivalent reactance becomes infinite. The SVC effective reactance X_{SVC} is determined by the parallel combination of X_C and X_{TCR} .

$$X_{SVC} = \frac{\pi XLXC}{XC \{2(\pi - \alpha) + \sin 2\alpha\} - \pi XL}$$

where $X_C = \frac{1}{\omega C}$

$$Q_k = -V_k^2 \left\{ \frac{XC^2 (\pi - \alpha) + \sin 2\alpha}{\pi XCXL} \right\}$$

The SVC equivalent reactance is given above equation. It is shown in Fig. 2.2 that the SVC equivalent susceptance ($B_{SVC} = -1/X_{SVC}$) profile, as function of firing angle, does not present discontinuities, i.e., B_{SVC} varies in a continuous, smooth fashion in both operative regions. Hence, linearization of the SVC power flow equations based on B_{SVC} with respect to firing angle, will exhibit a better numerical behavior than the linearized model based on X_{SVC} .

3. Simulation results and discussions

The simulation results and discussion are presented in subsections as 3.2–3.6, respectively.

3.1. General

The software is written in MATPOWER 4.0b4 computing environment and applied on a 2.63 GHz Pentium IV personal computer

Table 3.2
IEEE-9 bus system without and with SVC (± 5 MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (-5 MVAR)	Voltage with SVC (+5 MVAR)
1	1.1	1.099	1.076
2	1.097	1.098	1.089
3	1.087	1.089	1.082
4	1.094	1.095	1.092
5	1.084	1.085	1.08
6	1.1	1.1	1.096
7	1.089	1.09	1.084
8	1.1	1.099	1.095
9	1.072	1.082	1.063

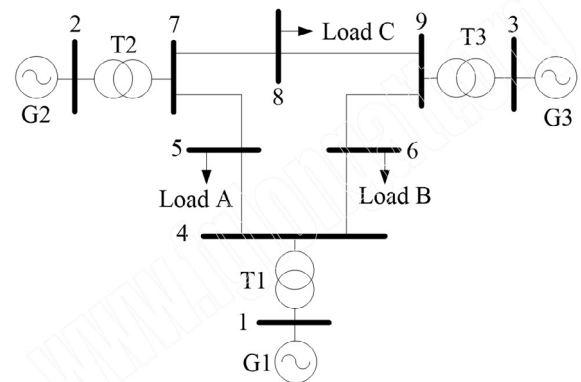


Fig. 3.1. Single line diagram of the IEEE 9 bus test system.

with 3 GB RAM. The simulation results and discussions corresponding to SVC tested on IEEE 9 and IEEE 30 bus system. Following representations are given below.

3.2. Test System 1: IEEE-9 bus system

The IEEE-9 bus test system and its data are given in Fig. 3.1 and Table 3.1, respectively.

In this test system there are 5 case studies with different size and location of SVC. Effects of SVC on Voltage profile are observed in this test system and also find out the optimal location of SVC. We use the Newton Raphson Load Flow method to calculate the bus voltage without SVC and with SVC.

3.2.1. Case study 1: IEEE-9 bus system with SVC (± 5 MVAR)

Fig. 3.2, it is observed that the voltage profile of the system has been improved after the placement of SVC. The overall voltage profile of the system has been improved when the SVC placed at bus no. 2, 3, 5, 7 and 9 but the improvement in voltage profile with maximum deviation is observed only at bus no. 9 (see Table 3.2).

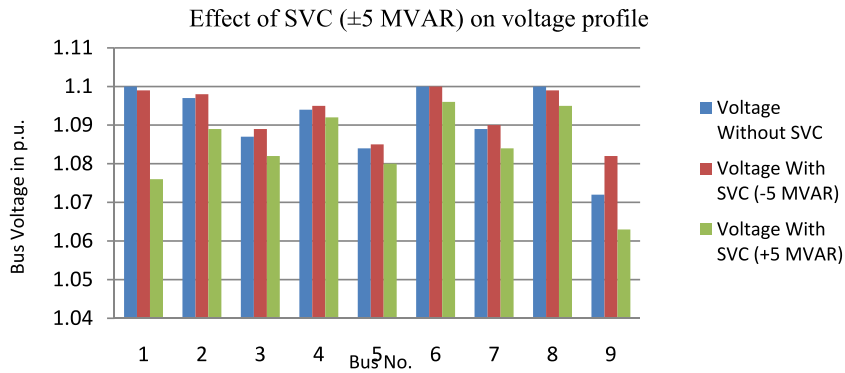


Fig. 3.2. Without and with SVC (±5 MVAR).

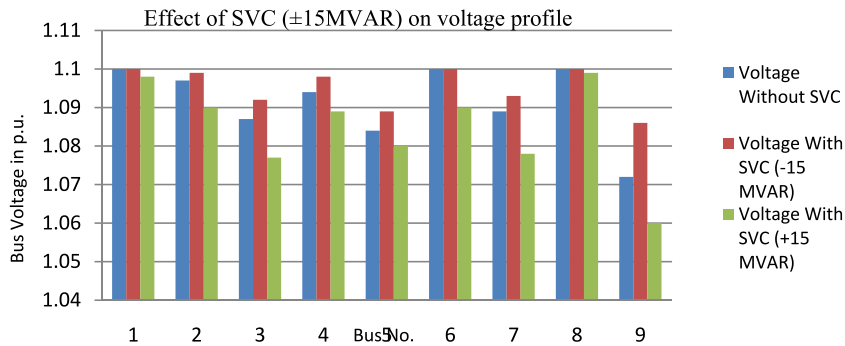


Fig. 3.3. Without and with SVC (±15 MVAR).

Table 3.3 IEEE-9 bus system without and with SVC (± 15 MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (-15 MVAR)	Voltage with SVC (+15 MVAR)
1	1.1	1.1	1.098
2	1.097	1.099	1.09
3	1.087	1.092	1.077
4	1.094	1.098	1.089
5	1.084	1.089	1.08
6	1.1	1.1	1.09
7	1.089	1.093	1.078
8	1.1	1.1	1.099
9	1.072	1.086	1.06

Table 3.4 IEEE-9 bus system without and with SVC (± 25 MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (-25 MVAR)	Voltage with SVC (+25 MVAR)
1	1.1	1.093	1.09
2	1.097	1.099	1.093
3	1.087	1.091	1.084
4	1.094	1.099	1.08
5	1.084	1.09	1.08
6	1.1	1.1	1.093
7	1.089	1.094	1.078
8	1.1	1.099	1.089
9	1.072	1.089	1.052

3.2.2. Case study 2: IEEE-9 bus system with SVC (±15 MVAR)

From Fig. 3.3, it is observed that the voltage profile of the system has been improved after the placement of SVC. The overall Voltage profile of the system has been improved when the SVC placed at bus no. 2, 3, 4, 5, 7 and 9 but the improvement in voltage profile with maximum deviation is observed only at bus no. 9 (see Table 3.3).

3.2.3. Case study 3: IEEE-9 bus system with SVC (±25 MVAR)

From Fig. 3.4, it is observed that the voltage profile of the system has been improved after the placement of SVC. The overall Voltage profile of the system has been improved when the SVC placed at bus no. 2, 3, 4, 5, 7 and 9 but the improvement in voltage profile with maximum deviation is observed only at bus no. 9 (see Table 3.4).

3.2.4. Case study 4: IEEE-9 bus system with SVC (± 35 MVAR)

From comparison in Fig. 3.5, it is observed that the voltage profile of the system has been improved after the placement of SVC. The overall Voltage profile of the system has been improved when the SVC placed at bus no. 2, 3, 4, 5, 7 and 9 but the improvement in

Table 3.5 IEEE-9 bus system without and with SVC (± 35 MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (-35 MVAR)	Voltage with SVC (+35 MVAR)
1	1.1	1.098	1.095
2	1.097	1.099	1.091
3	1.087	1.095	1.091
4	1.094	1.097	1.084
5	1.084	1.09	1.078
6	1.1	1.1	1.09
7	1.089	1.093	1.087
8	1.1	1.1	1.095
9	1.072	1.09	1.043

voltage profile with maximum deviation is observed only at bus no.9. Therefore the optimal location of SVC is at bus no. 9 (see Table 3.5).

3.2.5. Case study 5: IEEE-9 bus system with SVC (± 45 MVAR)

From comparison in Fig. 3.6, it is observed that the voltage profile of the system has been improved after the placement of SVC. The overall voltage profile of the system has been improved when

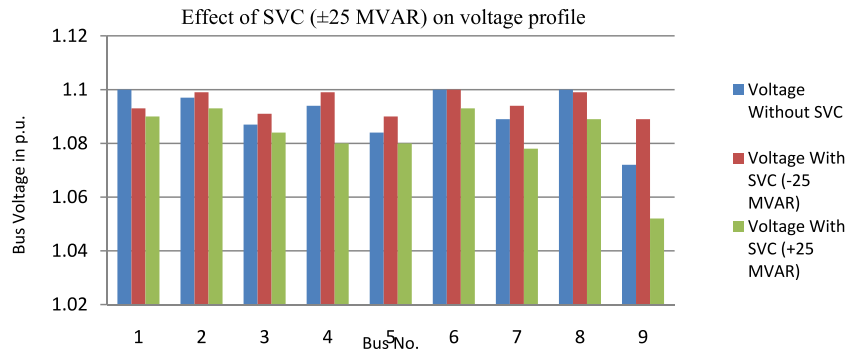


Fig. 3.4. Without and with SVC (±25 MVAR).

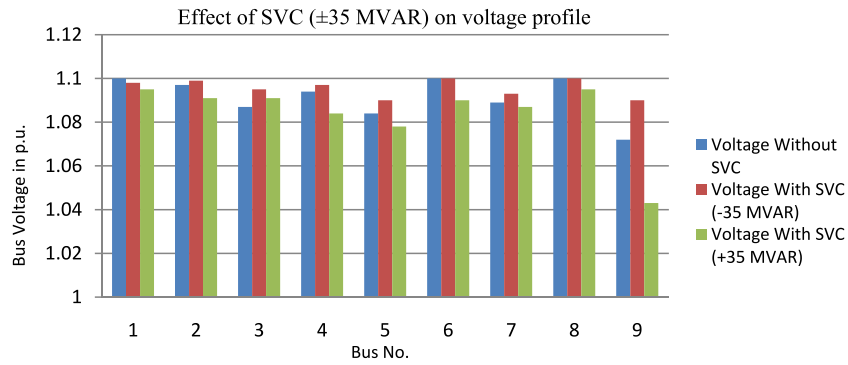


Fig. 3.5. Without and with SVC (±35 MVAR).

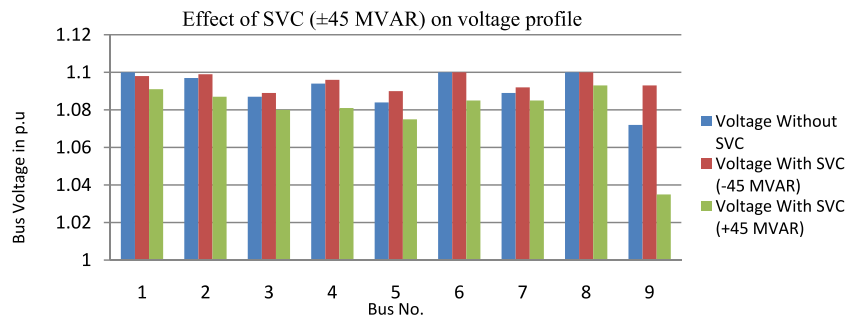


Fig. 3.6. Without and with SVC (±45 MVAR).

Table 3.6
IEEE-9 bus system without and with SVC (± 45 MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (-45 MVAR)	Voltage with SVC (+45 MVAR)
1	1.1	1.098	1.091
2	1.097	1.099	1.087
3	1.087	1.089	1.08
4	1.094	1.096	1.081
5	1.084	1.09	1.075
6	1.1	1.1	1.085
7	1.089	1.092	1.085
8	1.1	1.1	1.093
9	1.072	1.093	1.035

the SVC placed at bus no. 2, 3, 4, 5, 7 and 9 but the improvement in voltage profile with maximum deviation is observed only at bus no. 9. Therefore the optimal location of SVC is at bus no. 9 (see Table 3.6).

3.3. Comprehensive result analysis for voltage profile

In IEEE-9 bus system the result of voltage profile has been improved after the placement of SVC. From the above mentioned

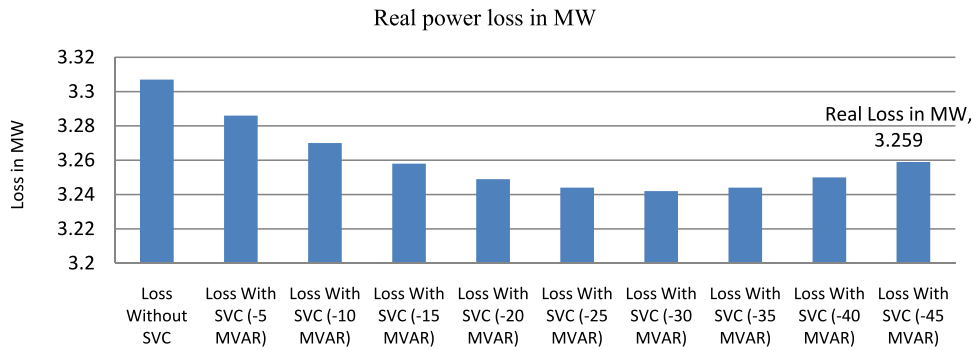


Fig. 3.7. Graphical comparisons between all the results of real power loss in IEEE-9 bus system without and with SVC (–ve MVAR).

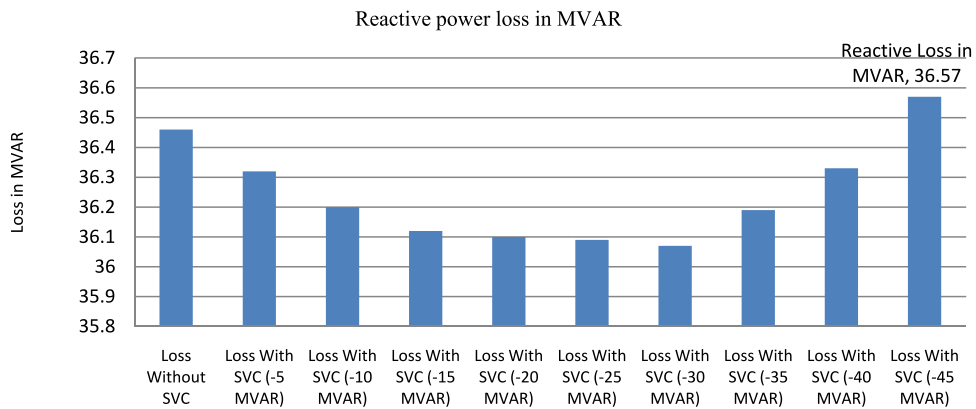


Fig. 3.8. Graphical comparisons between all the results of reactive power loss in IEEE-9 bus system without and with SVC (–ve MVAR).

Table 3.7

Cumulative voltage profile without and with SVC (–ve MVAR).

Bus no.	V Wo SVC	V W SVC (-5 MVAR)	V W SVC (-10 MVAR)	V W SVC (-15 MVAR)	V W SVC (-20 MVAR)	V W SVC (-25 MVAR)	V W SVC (-30 MVAR)	V W SVC (-35 MVAR)	V W SVC (-40 MVAR)	V W SVC (-45 MVAR)
1	1.1	1.099	1.098	1.1	1.097	1.093	1.096	1.098	1.098	1.098
2	1.097	1.098	1.099	1.099	1.094	1.099	1.099	1.099	1.099	1.099
3	1.087	1.089	1.09	1.092	1.092	1.091	1.092	1.095	1.095	1.089
4	1.094	1.095	1.094	1.098	1.095	1.099	1.098	1.097	1.097	1.096
5	1.084	1.085	1.087	1.089	1.09	1.09	1.089	1.09	1.09	1.09
6	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
7	1.089	1.09	1.093	1.093	1.09	1.094	1.094	1.093	1.094	1.092
8	1.1	1.099	1.1	1.1	1.1	1.099	1.1	1.1	1.1	1.1
9	1.072	1.082	1.085	1.086	1.088	1.089	1.089	1.09	1.091	1.093

case studies the overall data of analytical studies of voltage profile without and with SVC is collected and a cumulative voltage profile presented in Table 3.7 for IEEE-9 bus system without and with SVC feeding negative and positive MVAR respectively.

From graphical comparison shown below in Fig. 3.10, it is observed that the voltage profile of the system has been improved after the placement of SVC. The overall Voltage profile of the system has been improved when the SVC placed but the improvement in voltage profile with maximum deviation is observed only at bus no. 9. Therefore the optimal location is at bus no. 9 and the optimal size is –30 MVR.

3.4. Comprehensive result analysis: Real and reactive power loss without and with SVC

From comparison in Fig. 3.7, it is observed that the real power loss of the system has been reduced after the placement of SVC. The overall real power loss of the system has been decreased with increase the size of SVC till –30 MVR after that real power loss

increases again. Therefore the optimal location is at bus no. 9 and the optimal size is –30 MVR (see Table 3.8).

From comparison in Fig. 3.8, it is observed that the reactive power loss of the system has been reduced after the placement of SVC. The overall reactive power loss of the system has been decreased with increase the size of SVC till –30 MVR after that reactive power loss increases again. Therefore the optimal location is at bus no. 9 and the optimal size is –30 MVR (see Table 3.9).

From comparison shown in Fig. 3.9, it is concluded that when the size of SVC is increasing real power loss is also increasing, in other words with the injection of SVC (+ve MVAR) real power losses increases.

From comparison shown in Fig. 3.10 it is concluded that when the size of SVC has been increased Reactive Power loss is also increased, in other words with the injection of SVC (+ve MVAR) Reactive Power losses increases.

3.5. Comprehensive result analysis: Cost profile with and without SVC

In IEEE-9 bus system the result of voltage profile has been improved after the placement of SVC. From the above mentioned

Table 3.8
Cumulative real and reactive power loss of without and with SVC (–ve MVAR).

Power loss	Loss Wo SVC	Loss with SVC (–5 MVAR)	Loss with SVC (–10 MVAR)	Loss with SVC (–15 MVAR)	Loss with SVC (–20 MVAR)	Loss with SVC (–25 MVAR)	Loss with SVC (–30 MVAR)	Loss with SVC (–35 MVAR)	Loss with SVC (–40 MVAR)	Loss with SVC (–45 MVAR)
Real loss (MW)	3.307	3.286	3.27	3.258	3.249	3.244	3.242	3.244	3.25	3.259
Reactive loss (MVAR)	36.46	36.32	36.2	36.12	36.1	36.09	36.07	36.19	36.33	36.57

Table 3.9
Cumulative real and reactive power loss of without and with SVC (+ve MVAR).

Power loss	Loss Wo SVC	Loss with SVC (+5 MVAR)	Loss with SVC (+10 MVAR)	Loss with SVC (+15 MVAR)	Loss with SVC (+20 MVAR)	Loss with SVC (+25 MVAR)	Loss with SVC (+30 MVAR)	Loss with SVC (+35 MVAR)	Loss with SVC (+40 MVAR)	Loss with SVC (+45 MVAR)
Real loss (MW)	3.307	3.332	3.363	3.402	3.446	3.495	3.55	3.611	3.678	3.751
Reactive loss (MVAR)	36.46	36.64	36.86	37.15	37.5	37.89	38.33	38.82	39.37	39.97

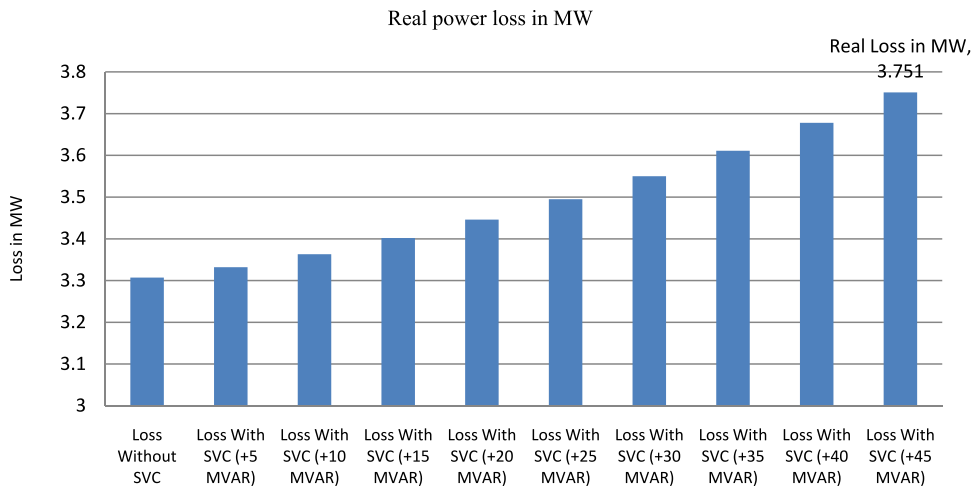


Fig. 3.9. Graphical comparisons between all the results of real power loss in IEEE-9 bus system without and with SVC (+ve MVAR).

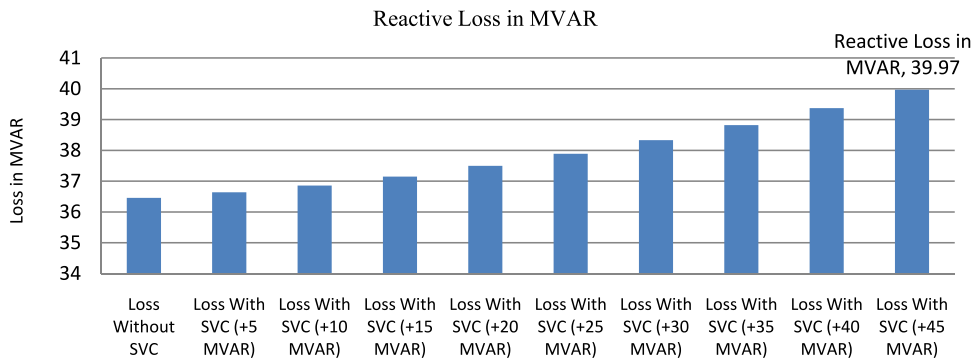


Fig. 3.10. Graphical comparisons between all the results of reactive power loss in IEEE-9 bus system without and with SVC (+ve MVAR).

case studies the overall data of analytical studies of cost profile without and with SVC is collected and a cumulative cost profile presented in Table 3.10 for IEEE-9 bus system without and with SVC feeding negative and positive MVAR respectively.

From comparison shown in Fig. 3.11, it is concluded that when the size of SVC (–ve MVAR) is increasing Real cost for IEEE-9 bus system is decreasing till its optimal location i.e. –30 MVAR after that Real cost increases again.

From comparison shown in Fig. 3.12, it is concluded that when the size of SVC (–ve MVAR) is increasing Reactive cost for IEEE-9 bus system is decreasing continuously.

3.6. Test system 2: IEEE-30 bus system

The IEEE-30 bus test system and its data are given in Fig. 3.13 and Table 3.11, respectively.

In this test system there are 5 case studies with different size and location of SVC. Effects of SVC on Voltage profile are observed in this test system and also find out the optimal location of SVC.

3.6.1. Case study 1: IEEE-30 bus system with SVC (±5 MVAR)

From comparison in Fig. 3.14, it is observed that the voltage profile of the system has been improved after the placement of

Table 3.10
Cost of IEEE-9 bus system without and with SVC (–ve MVAR).

Cost	Cost Wo SVC	Cost with SVC (–5 MVAR)	Cost with SVC (–10 MVAR)	Cost with SVC (–15 MVAR)	Cost with SVC (–20 MVAR)	Cost with SVC (–25 MVAR)	Cost with SVC (–30 MVAR)	Cost with SVC (–35 MVAR)	Cost with SVC (–40 MVAR)	Cost with SVC (–45 MVAR)
Real power cost	219.985	219.965	219.955	219.944	219.935	219.931	219.923	219.926	219.929	219.932
Reactive power cost	0.179	0.15	0.13	0.112	0.094	0.078	0.062	0.044	0.027	0.012

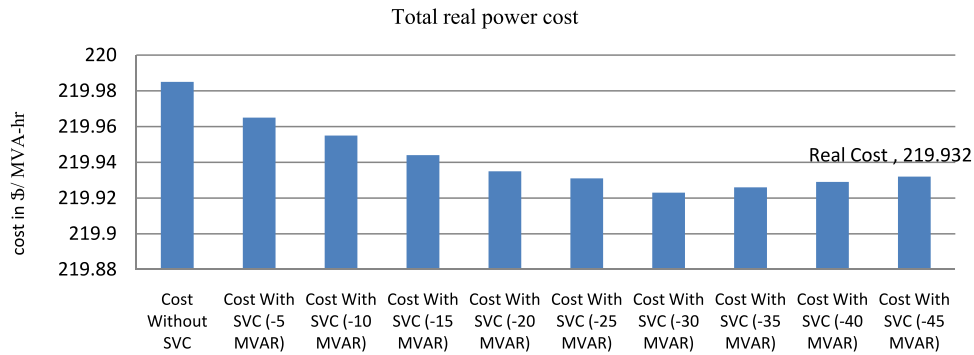


Fig. 3.11. Real cost profile for IEEE-9 bus system without and with SVC (–ve MVAR).

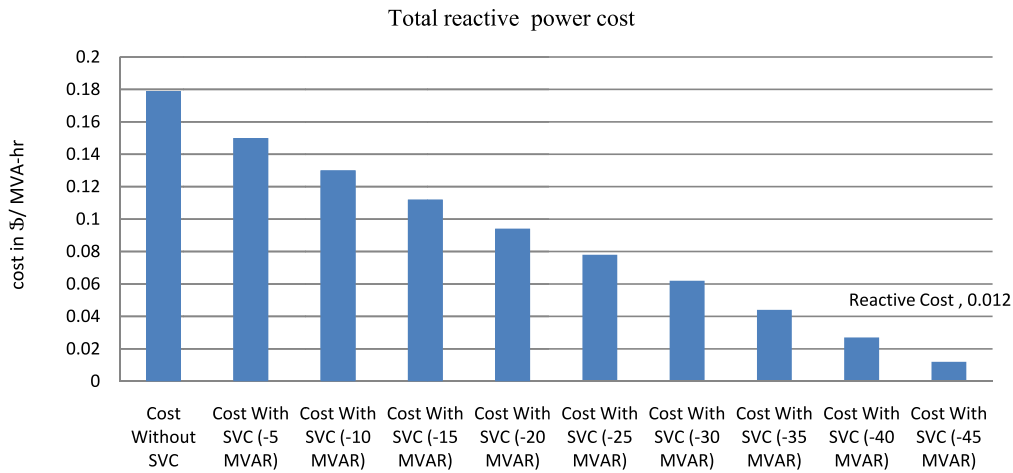


Fig. 3.12. Reactive cost profile for IEEE-9 bus system without and with SVC (–ve MVAR).

SVC. The overall Voltage profile of the system has been improved when the SVC placed but the improvement in voltage profile with maximum deviation is observed at bus no. 8. Therefore the optimal location of SVC is at bus no. 8 (see Table 3.12).

3.6.2. Case study 2: IEEE-30 bus system with SVC (±15 MVAR)

From comparison in Fig. 3.15, it is observed that the voltage profile of the system has been improved after the placement of SVC. The overall Voltage profile of the system has been improved when the SVC placed but the improvement in voltage profile with maximum deviation is observed at bus no. 8 (see Table 3.13).

3.6.3. Case study 3: IEEE-30 bus system with SVC (±25 MVAR)

From comparison in Fig. 3.16, it is observed that the voltage profile of the system has been improved after the placement of SVC. The overall Voltage profile of the system has been improved when the SVC placed but the improvement in voltage profile with maximum deviation is observed at bus no. 8 (see Table 3.14).

3.6.4. Case study 4: IEEE-30 bus system with SVC (±35 MVAR)

From comparison in Fig. 3.17, it is observed that the voltage profile of the system has been improved after the placement of SVC. The overall Voltage profile of the system has been improved when the SVC placed but the improvement in voltage profile with maximum deviation is observed at bus no. 8 (see Table 3.15).

3.6.5. Case study 5: IEEE-30 bus system with SVC (±45 MVAR)

From comparison in Fig. 3.18, it is observed that the voltage profile of the system has been improved after the placement of SVC and maximum deviation is observed at bus no. 8 (see Table 3.16).

3.7. Comprehensive result analysis: Voltage profile of IEEE-30 bus system

In IEEE-30 bus system the result of voltage profile has been improved after the placement of SVC. From the above mentioned case studies the overall data of analytical studies of voltage profile

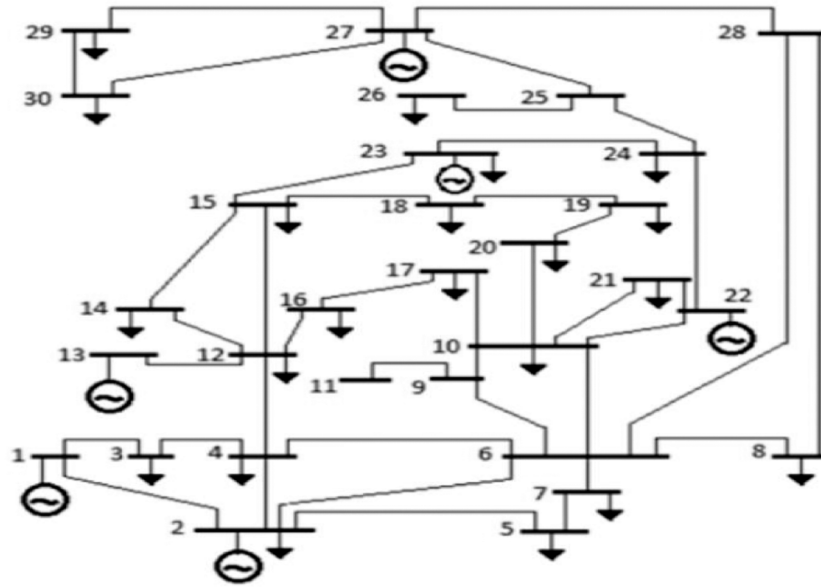


Fig. 3.13. Single line diagram of the IEEE 30 bus test system.

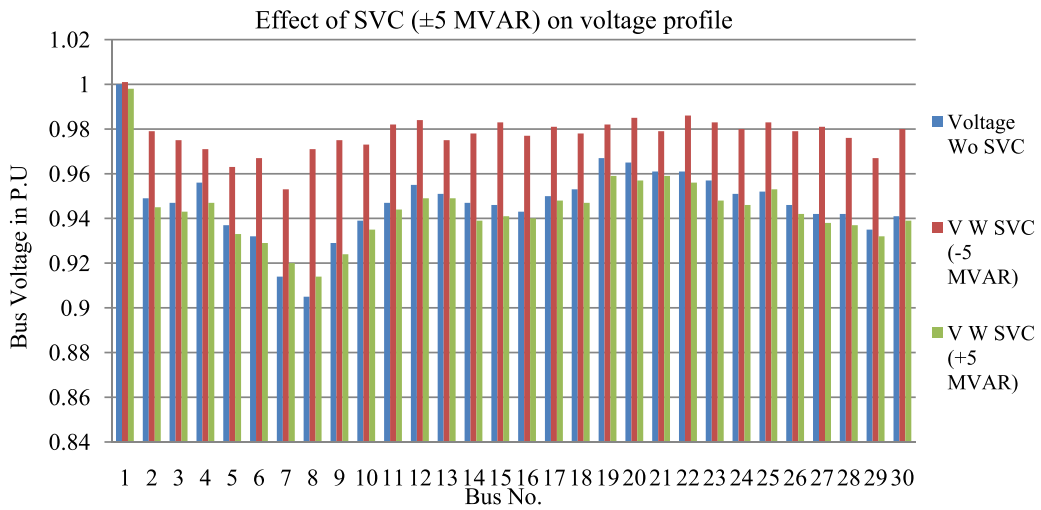


Fig. 3.14. Without and with SVC (±5 MVAR).

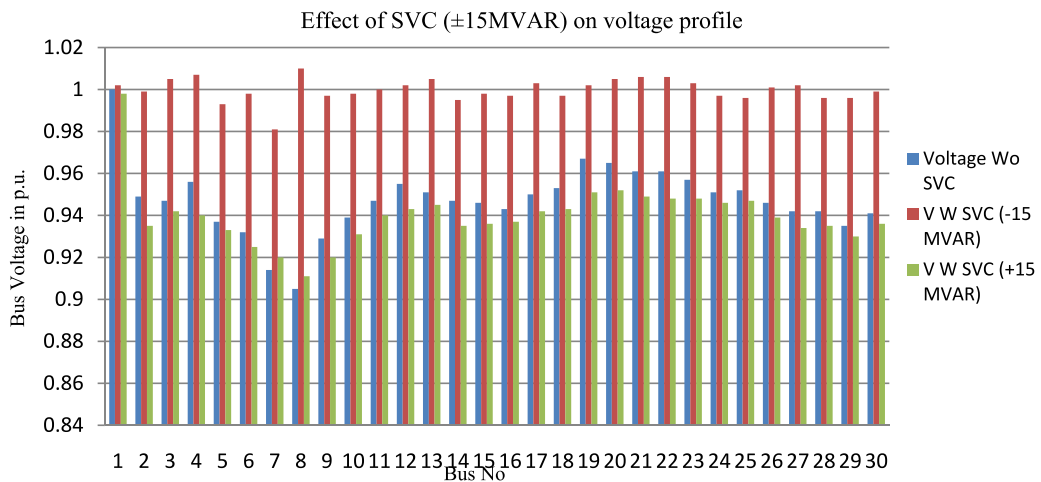


Fig. 3.15. Without and with SVC (±15 MVAR).

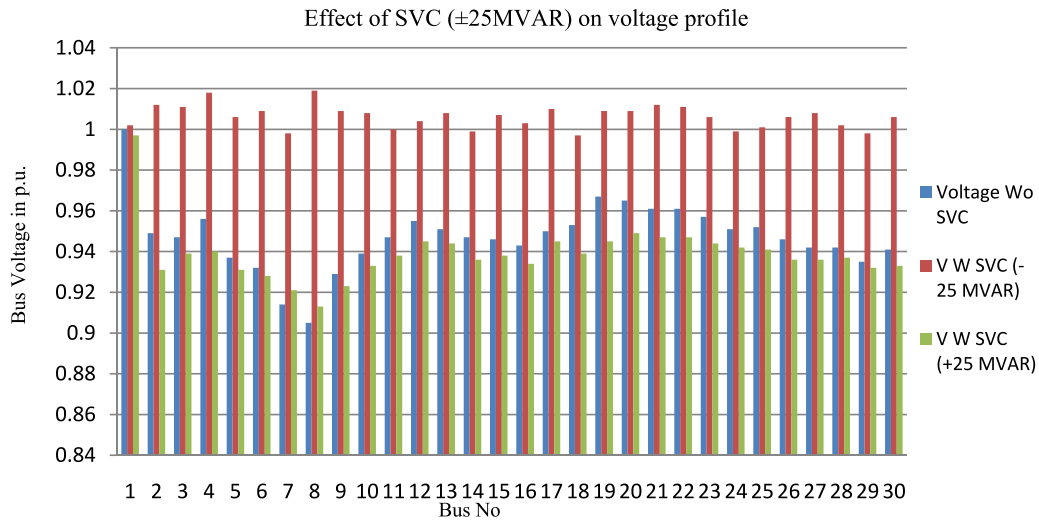


Fig. 3.16. Without and with SVC (± 25 MVAR).

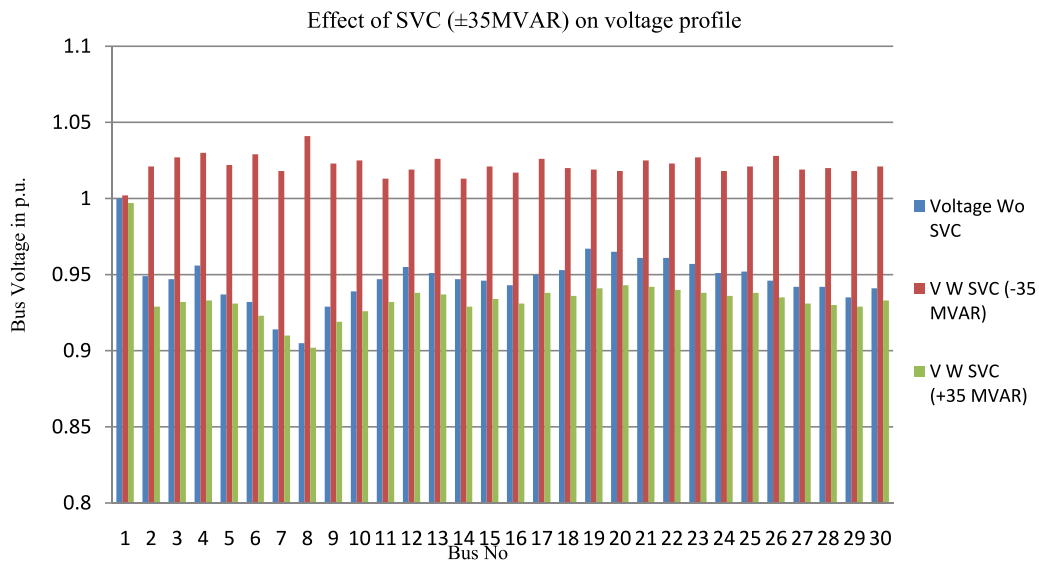


Fig. 3.17. Without and with SVC (± 35 MVAR).

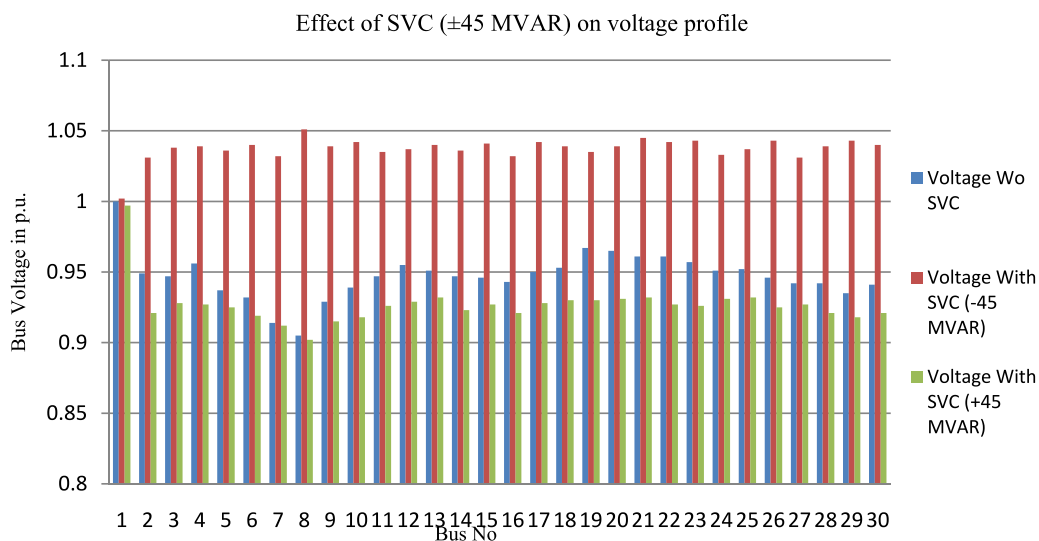


Fig. 3.18. Without and with SVC (± 45 MVAR).

Table 3.11
Parameters of IEEE 30 bus system.

Line No	Bus		Impedance		Shunt susceptance
	From	To	Resistance	Reactance	
1	1	2	0.0200	0.0600	0.0300
2	1	3	0.0500	0.1900	0.0200
3	2	4	0.0600	0.1700	0.0200
4	3	4	0.0100	0.0400	0
5	2	5	0.0500	0.2000	0.0200
6	2	6	0.0600	0.1800	0.0200
7	4	6	0.0100	0.0400	0
8	5	7	0.0500	0.1200	0.0100
9	6	7	0.0300	0.0800	0.0100
10	6	8	0.0100	0.0400	0
11	6	9	0	0.2100	0
12	6	10	0	0.5600	0
13	9	11	0	0.2100	0
14	9	10	0	0.1100	0
15	4	12	0	0.2600	0
16	4	13	0	0.1400	0
17	12	14	0.1200	0.2600	0
18	12	15	0.0700	0.1300	0
19	12	16	0.0900	0.2000	0
20	14	15	0.2200	0.2000	0
21	16	17	0.0800	0.1900	0
22	15	18	0.1100	0.2200	0
23	18	19	0.6000	0.1300	0
24	19	20	0.0300	0.7000	0
25	10	20	0.0900	0.2100	0
26	10	17	0.0300	0.0800	0
27	10	21	0.0300	0.0700	0
28	10	22	0.7000	0.1500	0
29	21	22	0.0100	0.0200	0
30	15	23	0.0100	0.2000	0
31	22	24	0.1200	0.1800	0
32	23	24	0.1300	0.2700	0
33	24	25	0.1900	0.3300	0
34	25	26	0.2500	0.3800	0
35	25	27	0.1100	0.2100	0
36	28	27	0	0.4000	0
37	27	29	0.2200	0.4200	0
38	27	30	0.3200	0.6000	0
39	29	30	0.2400	0.4500	0
40	8	28	0.0600	0.2000	0.0200
41	9	28	0.0200	0.0600	0.0100

without and with SVC is collected and a cumulative voltage profile presented in Tables 3.17 and 3.18 for IEEE-30 bus system without and with SVC feeding negative.

3.8. Comprehensive result analysis: Real and reactive power loss without and with SVC

The comprehensive result analysis of real and reactive power loss profile in IEEE-30 bus system are given below in Table 3.19. This table shows the real and reactive power loss profile of the buses with and without SVC. The overall real and reactive power loss profile of 30 bus system is minimized when SVC are placed at optimal location.

From comparison in Figs. 3.19 and 3.20, it is observed that the reactive power loss of the system has been reduced after the placement of SVC. The overall reactive power loss of the system has been decreased with increase the size of SVC till -35 MVAR after that reactive power loss increases again. Therefore the optimal location is at bus no. 8 and the optimal size is -35 MVAR (see Table 3.20).

From comparison shown in Fig. 3.21, it is concluded that when the size of SVC is increasing real power loss is also increasing, in other words with the injection of SVC (+ve MVAR) real power losses increases.

Table 3.12
IEEE-30 bus system without and with SVC (± 5 MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (-5 MVAR)	Voltage with SVC (+5 MVAR)
1	1	1.001	0.998
2	0.949	0.979	0.945
3	0.947	0.975	0.943
4	0.956	0.971	0.947
5	0.937	0.963	0.933
6	0.932	0.967	0.929
7	0.914	0.953	0.92
8	0.905	0.971	0.914
9	0.929	0.975	0.924
10	0.939	0.973	0.935
11	0.947	0.982	0.944
12	0.955	0.984	0.949
13	0.951	0.975	0.949
14	0.947	0.978	0.939
15	0.946	0.983	0.941
16	0.943	0.977	0.94
17	0.95	0.981	0.948
18	0.953	0.978	0.947
19	0.967	0.982	0.959
20	0.965	0.985	0.957
21	0.961	0.979	0.959
22	0.961	0.986	0.956
23	0.957	0.983	0.948
24	0.951	0.98	0.946
25	0.952	0.983	0.953
26	0.946	0.979	0.942
27	0.942	0.981	0.938
28	0.942	0.976	0.937
29	0.935	0.967	0.932
30	0.941	0.98	0.939

Table 3.13
IEEE-30 bus system without and with SVC (± 15 MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (-15 MVAR)	Voltage with SVC (+15 MVAR)
1	1	1.002	0.998
2	0.949	0.999	0.935
3	0.947	1.005	0.942
4	0.956	1.007	0.94
5	0.937	0.993	0.933
6	0.932	0.998	0.925
7	0.914	0.981	0.92
8	0.905	1.01	0.911
9	0.929	0.997	0.92
10	0.939	0.998	0.931
11	0.947	1	0.94
12	0.955	1.002	0.943
13	0.951	1.005	0.945
14	0.947	0.995	0.935
15	0.946	0.998	0.936
16	0.943	0.997	0.937
17	0.95	1.003	0.942
18	0.953	0.997	0.943
19	0.967	1.002	0.951
20	0.965	1.005	0.952
21	0.961	1.006	0.949
22	0.961	1.006	0.948
23	0.957	1.003	0.948
24	0.951	0.997	0.946
25	0.952	0.996	0.947
26	0.946	1.001	0.939
27	0.942	1.002	0.934
28	0.942	0.996	0.935
29	0.935	0.996	0.93
30	0.941	0.999	0.936

3.9. Comprehensive result analysis: Cost profile with and without SVC

In IEEE-30 bus system the result of voltage profile has been improved after the placement of SVC. The overall data for cost

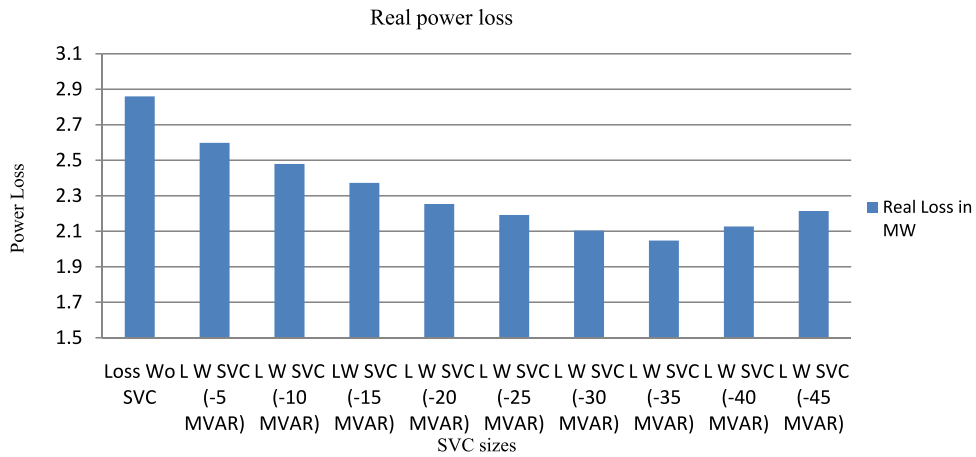


Fig. 3.19. Comparisons between all the results of real power loss in IEEE-30 bus system without and with SVC (–ve MVAR).

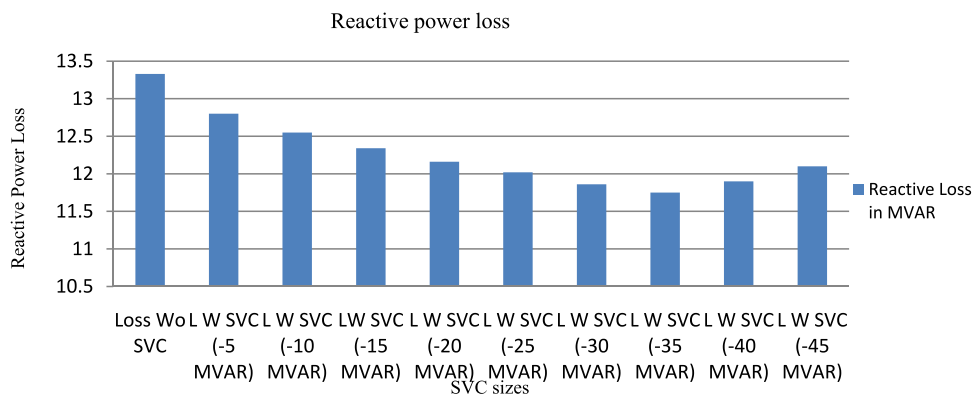


Fig. 3.20. Comparisons between all the results of reactive power loss in IEEE-30 bus system without and with SVC (–ve MVAR).

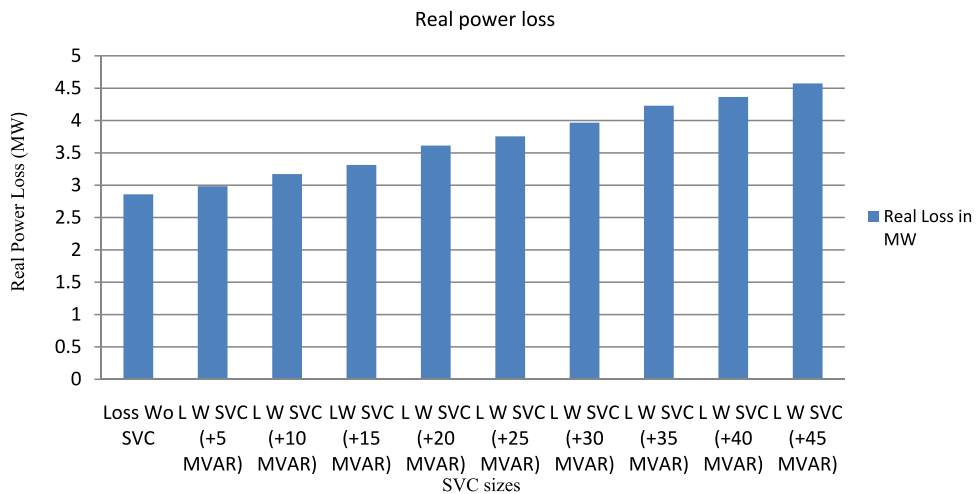


Fig. 3.21. Comparisons between all the results of Real Power loss in IEEE-30 bus system without and with SVC (+ve MVAR).

without and with SVC is collected and a cumulative voltage profile presented in Table 3.21 for IEEE-30 bus system without and with SVC feeding negative and positive MVAR respectively.

From Comparisons shown in Figs. 3.22 and 3.23 it is concluded that when the size of SVC (–ve MVAR) is increasing real and reactive cost for IEEE-30 bus system is decreasing continuously till the size of –35 MVAR i.e. the optimal size, after that the cost further increases.

4. Conclusions and futurescope of research work

The conclusions and future scope of research work are addressed in Sections 4.1–4.2, respectively.

4.1. Conclusions

The following conclusions made from this research work are as follows:

Table 3.14
IEEE-30 bus system without and with SVC (± 25 MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (-25 MVAR)	Voltage with SVC ($+25$ MVAR)
1	1	1.002	0.997
2	0.949	1.012	0.931
3	0.947	1.011	0.939
4	0.956	1.018	0.94
5	0.937	1.006	0.931
6	0.932	1.009	0.928
7	0.914	0.998	0.921
8	0.905	1.019	0.913
9	0.929	1.009	0.923
10	0.939	1.008	0.933
11	0.947	1	0.938
12	0.955	1.004	0.945
13	0.951	1.008	0.944
14	0.947	0.999	0.936
15	0.946	1.007	0.938
16	0.943	1.003	0.934
17	0.95	1.01	0.945
18	0.953	0.997	0.939
19	0.967	1.009	0.945
20	0.965	1.009	0.949
21	0.961	1.012	0.947
22	0.961	1.011	0.947
23	0.957	1.006	0.944
24	0.951	0.999	0.942
25	0.952	1.001	0.941
26	0.946	1.006	0.936
27	0.942	1.008	0.936
28	0.942	1.002	0.937
29	0.935	0.998	0.932
30	0.941	1.006	0.933

Table 3.16
IEEE-30 bus system without and with SVC (± 45 MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (-45 MVAR)	Voltage with SVC ($+45$ MVAR)
1	1	1.002	0.997
2	0.949	1.031	0.921
3	0.947	1.038	0.928
4	0.956	1.039	0.927
5	0.937	1.036	0.925
6	0.932	1.04	0.919
7	0.914	1.032	0.912
8	0.905	1.051	0.902
9	0.929	1.039	0.915
10	0.939	1.042	0.918
11	0.947	1.035	0.926
12	0.955	1.037	0.929
13	0.951	1.04	0.932
14	0.947	1.036	0.923
15	0.946	1.041	0.927
16	0.943	1.032	0.921
17	0.95	1.042	0.928
18	0.953	1.039	0.93
19	0.967	1.035	0.93
20	0.965	1.039	0.931
21	0.961	1.045	0.932
22	0.961	1.042	0.927
23	0.957	1.043	0.926
24	0.951	1.033	0.931
25	0.952	1.037	0.932
26	0.946	1.043	0.925
27	0.942	1.031	0.927
28	0.942	1.039	0.921
29	0.935	1.043	0.918
30	0.941	1.04	0.921

Table 3.15
IEEE-30 bus system without and with SVC (± 35 MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (-35 MVAR)	Voltage with SVC ($+35$ MVAR)
1	1	1.002	0.997
2	0.949	1.021	0.929
3	0.947	1.027	0.932
4	0.956	1.03	0.933
5	0.937	1.022	0.931
6	0.932	1.029	0.923
7	0.914	1.018	0.91
8	0.905	1.041	0.902
9	0.929	1.023	0.919
10	0.939	1.025	0.926
11	0.947	1.013	0.932
12	0.955	1.019	0.938
13	0.951	1.026	0.937
14	0.947	1.013	0.929
15	0.946	1.021	0.934
16	0.943	1.017	0.931
17	0.95	1.026	0.938
18	0.953	1.02	0.936
19	0.967	1.019	0.941
20	0.965	1.018	0.943
21	0.961	1.025	0.942
22	0.961	1.023	0.94
23	0.957	1.027	0.938
24	0.951	1.018	0.936
25	0.952	1.021	0.938
26	0.946	1.028	0.935
27	0.942	1.019	0.931
28	0.942	1.02	0.93
29	0.935	1.018	0.929
30	0.941	1.021	0.933

- Voltage profile of the IEEE-9 bus system has been improved from 1.072 to 1.093 after incorporation of SVC at bus no. 9.

- Voltage profile of the IEEE-30 bus system has been improved from 0.905 to 1.048 after incorporation of SVC at bus no. 8.
- In 9 bus system the optimal located bus no. is 9 and optimal size of the SVC is 30 ($-ve$ MVAR).
- In 30 bus system the optimal located bus no. is 8 and optimal size of the SVC is 35 ($-ve$ MVAR).
- Inject active and reactive power flow in power system network
- Real power loss and reactive power loss are minimized.
- Real and reactive power flow control capability.
- Power system performance will improve when we add the SVC.

4.2. Future scope of work

The following future scopes of this work are as follows:

- In future, with insertion of two or more FACTS controller can be used in coordinated manner to enhance voltage profile.
- In future, other member of FACTS controllers such as UPFC, HPFC etc. is also used improving voltage profile and minimizing the real and reactive power losses.
- In future, the Artificial Intelligence techniques are used for verification of OPF results and for better enhancement of voltage profile
- In future, the Hybrid Artificial Intelligence techniques are used for verification of OPF results and for better enhancement of voltage profile
- In future, other power system performances may be improved such as system power factor, power quality parameters (voltage sag and swell *etc.*) by optimally placed FACTS controllers with DGs.

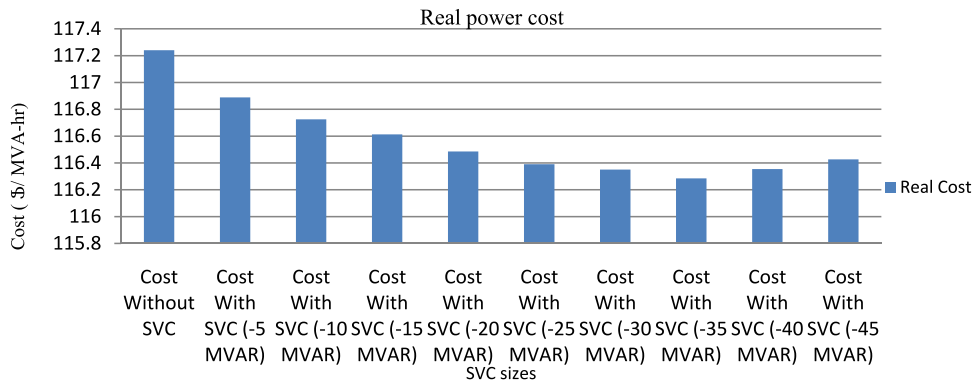


Fig. 3.22. Total real cost profile for IEEE-30 bus system without and with SVC (–ve MVAR).

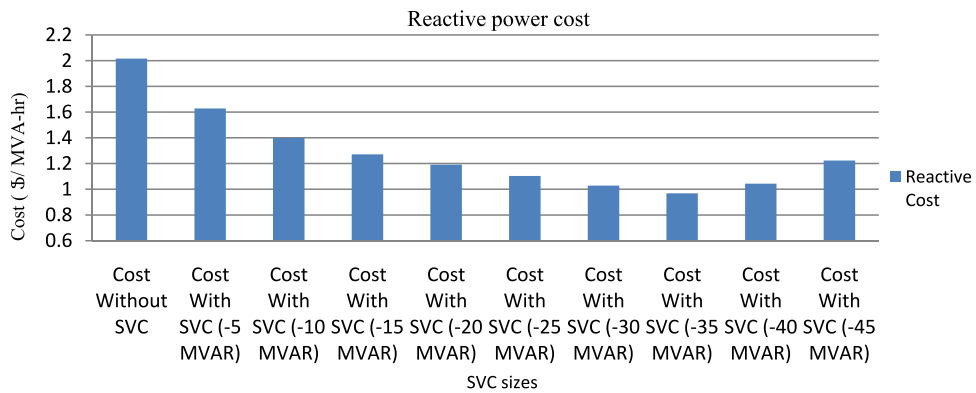


Fig. 3.23. Reactive cost profile for IEEE-30 bus system without and with SVC (–ve MVAR).

Table 3.17

Cumulative voltage profile of IEEE-30 bus system without and with SVC (–ve MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (-5 MVAR)	Voltage with SVC (-10 MVAR)	Voltage with SVC (-15 MVAR)	Voltage with SVC (-20 MVAR)	Voltage with SVC (-25 MVAR)	Voltage with SVC (-30 MVAR)	Voltage with SVC (-35 MVAR)	Voltage with SVC (-40 MVAR)	Voltage with SVC (-45 MVAR)
1	1	1.001	1.001	1.002	1.002	1.002	1.002	1.002	1.002	1.002
2	0.949	0.979	0.991	0.999	1.009	1.012	1.015	1.021	1.027	1.031
3	0.947	0.975	0.995	1.005	1.01	1.011	1.017	1.027	1.031	1.038
4	0.956	0.971	0.997	1.007	1.015	1.018	1.023	1.03	1.035	1.039
5	0.937	0.963	0.983	0.993	1.003	1.006	1.016	1.022	1.03	1.036
6	0.932	0.967	0.986	0.998	1.007	1.009	1.018	1.029	1.035	1.04
7	0.914	0.953	0.965	0.981	0.996	0.998	1.008	1.018	1.024	1.032
8	0.905	0.971	0.991	1.01	1.013	1.019	1.031	1.041	1.047	1.051
9	0.929	0.975	0.987	0.997	1.006	1.009	1.019	1.023	1.028	1.039
10	0.939	0.973	0.993	0.998	1.005	1.008	1.017	1.025	1.039	1.042
11	0.947	0.982	0.992	1	1.002	1	1.003	1.013	1.027	1.035
12	0.955	0.984	0.994	1.002	1.005	1.004	1.014	1.019	1.029	1.037
13	0.951	0.975	0.995	1.005	1.008	1.008	1.016	1.026	1.032	1.04
14	0.947	0.978	0.987	0.995	0.999	0.999	1.004	1.013	1.023	1.036
15	0.946	0.983	0.993	0.998	1.001	1.007	1.011	1.021	1.033	1.041
16	0.943	0.977	0.987	0.997	1.006	1.003	1.009	1.017	1.026	1.032
17	0.95	0.981	0.993	1.003	1.009	1.01	1.019	1.026	1.036	1.042
18	0.953	0.978	0.988	0.997	0.999	0.997	1.007	1.02	1.03	1.039
19	0.967	0.982	0.992	1.002	1.008	1.009	1.012	1.019	1.028	1.035
20	0.965	0.985	0.995	1.005	1.004	1.009	1.011	1.018	1.029	1.039
21	0.961	0.979	0.99	1.006	1.009	1.012	1.015	1.025	1.038	1.045
22	0.961	0.986	0.996	1.006	1.009	1.011	1.013	1.023	1.035	1.042
23	0.957	0.983	0.993	1.003	1.003	1.006	1.016	1.027	1.04	1.043
24	0.951	0.98	0.989	0.997	0.998	0.999	1.008	1.018	1.026	1.033
25	0.952	0.983	0.989	0.996	0.999	1.001	1.007	1.021	1.029	1.037
26	0.946	0.979	0.991	1.001	1.007	1.006	1.015	1.028	1.037	1.043
27	0.942	0.981	0.988	1.002	1.008	1.008	1.01	1.019	1.021	1.031
28	0.942	0.976	0.986	0.996	0.999	1.002	1.002	1.02	1.029	1.039
29	0.935	0.967	0.987	0.996	0.997	0.998	1	1.018	1.035	1.043
30	0.941	0.98	0.992	0.999	1.002	1.006	1.009	1.021	1.03	1.04

Table 3.18
Cumulative voltage profile of IEEE-30 bus system without and with SVC (+ve MVAR).

Bus no.	Voltage without SVC	Voltage with SVC (+5 MVAR)	Voltage with SVC (+10 MVAR)	Voltage with SVC (+15 MVAR)	Voltage with SVC (+20 MVAR)	Voltage with SVC (+25 MVAR)	Voltage with SVC (+30 MVAR)	Voltage with SVC (+35 MVAR)	Voltage with SVC (+40 MVAR)	Voltage with SVC (+45 MVAR)
1	1	0.998	0.998	0.998	0.998	0.997	0.997	0.997	0.997	0.997
2	0.949	0.945	0.939	0.935	0.934	0.931	0.931	0.929	0.925	0.921
3	0.947	0.943	0.944	0.942	0.94	0.939	0.937	0.932	0.93	0.928
4	0.956	0.947	0.942	0.94	0.941	0.94	0.939	0.933	0.931	0.927
5	0.937	0.933	0.935	0.933	0.932	0.931	0.936	0.931	0.928	0.925
6	0.932	0.929	0.927	0.925	0.922	0.928	0.925	0.923	0.921	0.919
7	0.914	0.92	0.92	0.92	0.92	0.921	0.92	0.91	0.91	0.912
8	0.905	0.914	0.911	0.911	0.914	0.913	0.912	0.902	0.901	0.902
9	0.929	0.924	0.922	0.92	0.925	0.923	0.921	0.919	0.918	0.915
10	0.939	0.935	0.93	0.931	0.936	0.933	0.931	0.926	0.92	0.918
11	0.947	0.944	0.941	0.94	0.939	0.938	0.936	0.932	0.927	0.926
12	0.955	0.949	0.945	0.943	0.948	0.945	0.942	0.938	0.931	0.929
13	0.951	0.949	0.946	0.945	0.944	0.944	0.941	0.937	0.932	0.932
14	0.947	0.939	0.934	0.935	0.938	0.936	0.934	0.929	0.924	0.923
15	0.946	0.941	0.938	0.936	0.939	0.938	0.937	0.934	0.928	0.927
16	0.943	0.94	0.94	0.937	0.936	0.934	0.934	0.931	0.926	0.921
17	0.95	0.948	0.946	0.942	0.939	0.945	0.94	0.938	0.931	0.928
18	0.953	0.947	0.946	0.943	0.942	0.939	0.942	0.936	0.932	0.93
19	0.967	0.959	0.954	0.951	0.949	0.945	0.944	0.941	0.937	0.93
20	0.965	0.957	0.953	0.952	0.951	0.949	0.947	0.943	0.936	0.931
21	0.961	0.959	0.955	0.949	0.948	0.947	0.945	0.942	0.935	0.932
22	0.961	0.956	0.953	0.948	0.947	0.947	0.944	0.94	0.934	0.927
23	0.957	0.948	0.948	0.948	0.947	0.944	0.942	0.938	0.931	0.926
24	0.951	0.946	0.947	0.946	0.945	0.942	0.94	0.936	0.937	0.931
25	0.952	0.953	0.951	0.947	0.944	0.941	0.941	0.938	0.932	0.932
26	0.946	0.942	0.941	0.939	0.938	0.936	0.935	0.935	0.931	0.925
27	0.942	0.938	0.935	0.934	0.939	0.936	0.933	0.931	0.93	0.927
28	0.942	0.937	0.934	0.935	0.938	0.937	0.934	0.93	0.927	0.921
29	0.935	0.932	0.933	0.93	0.933	0.932	0.93	0.929	0.922	0.918
30	0.941	0.939	0.938	0.936	0.935	0.933	0.935	0.933	0.929	0.921

Table 3.19
Cumulative real and reactive power loss of IEEE-30 bus system without and with SVC (–ve MVAR).

Power loss	Loss without SVC	Loss with SVC (–5 MVAR)	Loss with SVC (–10 MVAR)	Loss with SVC (–15 MVAR)	Loss with SVC (–20 MVAR)	Loss with SVC (–25 MVAR)	Loss with SVC (–30 MVAR)	Loss with SVC (–35 MVAR)	Loss with SVC (–40 MVAR)	Loss with SVC (–45 MVAR)
Real power loss (MW)	2.86	2.598	2.479	2.373	2.254	2.192	2.104	2.048	2.127	2.214
Reactive power loss (MVAR)	13.33	12.8	12.55	12.34	12.16	12.02	11.86	11.75	11.9	12.1

Table 3.20
Cumulative real and reactive power loss of IEEE-30 bus system without and with SVC (+ve MVAR).

Power loss	Loss without SVC	Loss with SVC (+5 MVAR)	Loss with SVC (+10 MVAR)	Loss with SVC (+15 MVAR)	Loss with SVC (+20 MVAR)	Loss with SVC (+25 MVAR)	Loss with SVC (+30 MVAR)	Loss with SVC (+35 MVAR)	Loss with SVC (+40 MVAR)	Loss with SVC (+45 MVAR)
Real power loss (MW)	2.86	2.984	3.173	3.313	3.612	3.756	3.966	4.23	4.364	4.574
Reactive power loss (MVAR)	13.33	13.96	14.46	14.95	15.23	15.72	15.98	16.12	16.45	16.83

Table 3.21
Cost of IEEE-30 bus system without and with SVC (–ve MVAR).

Cost	Cost without SVC	Cost with SVC (–5 MVAR)	Cost with SVC (–10 MVAR)	Cost with SVC (–15 MVAR)	Cost with SVC (–20 MVAR)	Cost with SVC (–25 MVAR)	Cost with SVC (–30 MVAR)	Cost with SVC (–35 MVAR)	Cost with SVC (–40 MVAR)	Cost with SVC (–45 MVAR)
Real cost	117.241	116.889	116.725	116.613	116.486	116.391	116.351	116.285	116.354	116.427
Reactive cost	2.016	1.628	1.399	1.271	1.191	1.103	1.028	0.968	1.043	1.223

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