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Article

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Research paper

Maximum efficiency of wind energy using novel Dynamic Voltage Restorer for DFIG based Wind Turbine

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ABSTRACT

Fault-tolerable capability of Doubly Fed Induction Generator (DFIG) against disturbance occurrence is recognized as Fault Ride-Through (FRT). With quick and accurate compensation potentiality of Dynamic Voltage Restorer (DVR) to retrieve the nominal PCC voltage, DFIG can safely follow its normal operation in the power system. Multi-Level Inverter (MLI) as the main part of DVR with unique responsibility of synthesizing the staircase sinusoidal voltage ascertains the performance and flexibility of DVR. In this paper a novel asymmetrical MLI structure based on Level Creator and H-bridge inverter is indwelt in DVR in order to providing the high quality voltage. To more augment the efficiency of DVR in dealing with FRT issue, it has been equipped with Brain Emotional Learning Based Intelligent Controller (BELBIC) based on Multi Objective Bees Algorithm (MOBA). So-called AMLI-BELBIC based DVR has been thoroughly appraised under different balanced and unbalanced voltage sags and swells so that FRT capability of DFIG to be appeared. To sum up, the relevant analytical expression along with the simulation results has transparently corroborated the performance of AMLI-BELBIC based DVR aimed to augment the FRT capability of DFIG.

1. Introduction

Due to great dependency of world commercial management on the fossil fuels and environmental affects, the considerable assiduity on eminent capacity of Renewable Energy Resources (RER) has been ever more extending. In accordance with the multifarious energy markets, Wind Turbine (WT) has turned to be as the predominant RER technology that has been commonly applied in the islanded power systems (Zeng et al., 2013; Lund and Munster, 2006). Between all kinds of WT technologies, the variable speed WTs outfitted by doubly fed induction generators (DFIGs) have been extensively applied in wind power generation with respect to their benefits such as: cost-effectiveness, power flow controllability and flexibility (Muller et al., 2002; Tazil et al., 2010). The most prominent challenge concern to DFIG is following its normal operation i.e., DFIG FRT capability in the times of disturbance occurrence. That is to say, any balanced and unbalanced voltage sag or swell induces the serious fluctuations in currents of stator and rotor, and accordingly damage the DFIG electrical system (Mwasilu et al., 2012; Zhong et al., 2012).

Many different appliances based on power electronics e.g. Crowbars, DC-link choppers, Fault Current Limiters (FCLs), Series Dynamic Resistor (SDR) and Flexible Alternative Current Transmission Systems (FACTSs) have been applied as yet, so that DFIG FRT capability to be augmented. All these protection appliances expect FACTS devices have merely undertaken the alleviation of the current fluctuations of rotor and stator via untying up the RSC circuit as well as restricting the DC-link voltage in disturbance duration (Vidal et al., 2013; Pannell et al., 2010). Hence, the reactive power is attracted from the networks with the result of severe voltage drop, as a consequence, the gearbox and shaft of DFIG would be under severe stress (Ibrahim et al., 2011).

Provided using FACTS devices, not only the PCC voltage of affected network is compensated, but also no protection device is required to be indwelt in the interior circuit of DFIG systems (Wessels et al., 2011). DVR as high effective custom power or D-FACTS is here introduced to compensate the disturbed PCC voltage aimed to augment the FRT capability of DFIG. The major cost-price percentage of DVR is related to the three-phase voltage synthesizer. More number of embedded switches in MLI structure provides a staircase sinusoidal voltage with high-levels, i.e., high quality voltage (Barakati et al., 2008). The first MLI topology was introduced by Nabae et al. (1981). More requests have been thenceforth received by industrial companies that scientific scholars have responded to them by introducing pertinent MLI topologies (Rodriguez et al., 2002, 2007; Franquelo et al., 2008).

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Nomenclature

DFIG	Doubly Fed Induction Generator
DVR	Dynamic Voltage Restorer
FRT	Fault Ride-Through
MOBA	Multi Objective Bees Algorithm
PCC	Point of Common Coupling
AMLI	Asymmetrical Multi-Level Inverter
FO	Fractional Order
WT	Wind Turbine
RER	Renewable Energy Resource
THD	Total Harmonic Distortion
PWM	Pulse Width Modulation
PIV	Peak Inverse Voltage
SPL	Switching Power Losses
EMI	Electro-Magnetic Interference
MOBA	Multi Objective Bees Algorithm
NDS	Non-Dominated Sorting
HVDC	High Voltage Direct Current
FACTS	Flexible AC Transmission Systems
UPS	Uninterruptible Power Supply
PV	Photovoltaic
CHB	Cascaded H-Bridge
NPC	Neutral Point Clamped
FC	Flying Capacitor
FLC	Fuzzy Logic Control
ANFIS	Adaptive Neuro-Fuzzy Inference Systems
SMC	Sliding Mode Control
BELBIC	Brain Emotional Learning Based Intelligent Controller
PD	Phase Dissipation
POD	Phase Opposition Dissipation
APOD	Alternative Phase Opposition Dissipation
ST	Saw Tooth
PSC	Phase Shifted Carrier

Low switching losses, *PIV*, dV/dt and *EMI* are the strongpoints of MLI structures that let them to be occupied in higher voltage-levels (Meynard et al., 2002; Du et al., 2009; Sano and Fujita, 2008; Song et al., 2009). As a general, MLIs are classified into three categories viz. CHB, NPC, FC. Substantial drawback of these kinds of MLIs is incorporation a number of components e.g. switches, capacitors, diodes and suchlike aimed at providing a staircase sinusoidal voltage with high-levels. Up to now, several MLI structures with reduced switch numbers have been emerged to enhance the voltage quality with respect to low switch numbers (Adam et al., 2011; Liu et al., 2013; Yongdong et al., 2010). High number of switches will follow such these repercussions: complexity of circuit along with its pertinent control approach, growth of structure's cost-price, reduction of reliability, and maintenance of structure. In this regard, it would be practically impressive that the number of switches to be reduced that aimed to this subject several innovative and improved MLIs with reduced switches are introduced so that their relevant problems to be solved (Banaei and Salary, 2011b; Babaei et al., 2007; Banaei and Salary, 2011a). As to the performed attempts in this regard, a new MLI is suggested in this paper so that not only the number of switches to be reduced, but also a staircase sinusoidal voltage with high level to attained. The proposed asymmetrical MLI is constructed based on Level Creator and H-bridge inverter that the values of sub-MLIs DC sources have followed up special exponential form to create positive levels, then, the zero and negative levels have been created by H-bridge inverter. The configuration of the suggested AMLI enable it to provide a high level staircase sinusoidal voltage with low switch number as compared to other popular and innovative AMLI structures. Following that, it is indwelt in DVR in order to providing the high quality voltage.

To control the three-phase voltage synthesizer part, an effectual and robust controller must be brought in service of DVR control system so that a required voltage with high quality to be injected. In recent decades, several popular and innovative controllers e.g. PID, FLC, ANFIS, SMC, H∞ and the same have been utilized in different scientific applications in related to FACTS devices (Liu et al., 2016; Khuntia and Panda, 2013; Truong and Ngo, 2015). Brain Emotional Learning Based Intelligent Controller (BELBIC) is a recent effectual and robust approach based on a computational model of human brain emotional learning. Due to several advantages of BELBIC e.g. exoteric configuration, free model, high flexibility and the like, it has been successfully utilized in several scientific researches (Soreshjani et al., 2015a; Khalghani et al., 2016; Sadeghieha et al., 2012; Bijami et al., 2011). As for the particular characteristics of BELBIC, it is here considered that to be brought in service of DVR control system. Due to multi-objective nature of under-study problem, an efficacious multi objective optimization has been simultaneously implemented aimed at providing the optimal AMLI-BELBIC based DVR. Thus, exceptional performance of MOBA had created a stimulus to utilize it in order to solve the optimization problem.

So-called AMLI-BELBIC based DVR is indwelt in series of transmission line to augment the FRT capability of DFIG via compensating balanced and unbalanced voltage sags and voltage swells. As a result, DFIG can follow its normal operation as demanded in its grid code. To verify and validate the robustness of suggested DVR, it has been scrutinized under different fault types. Eventually, the relevant analytical expression along with the simulation results has transparently corroborated the performance of AMLI-BELBIC based DVR aimed to augment the FRT capability of DFIG. Other sections are here organized. Section 2: FRT problem of DFIG. Section 3: analysis, operation and comparison of the suggested multilevel inverter. Section 4: design and construction of BELBIC. Section 5: optimal design od AMLI-BELBIC based DVR using MOBA, Section 6: FRT capability of DFIG under different disturbances, Section 7: conclusion.

2. Doubly Fed Induction Generator

The single line diagram of under-study power system with presence of suggested DVR is given in Fig. 1(a). This power system has been constructed by 10 MVA DFIG-farm that is transferring the power to the infinite bus via step-up transformers and transmission lines. *AMLI-BELBIC based DVR* is indwelt in series of transmission line aimed to augment the FRT capability of DFIG via retrieving the affected voltage at DFIG junction bus into pre-fault state.

2.1. Fault Ride Through capability of DFIG

FRT is nowadays turned to be as the most outstanding issue related to the Renewable Energy Generation especially DFIG. FRT characteristic is prescribed by ascending or plunging the voltage at Point of Common Coupling (PCC) throughout fault incident then accordingly followed by a ramping down or up to the nominal level of voltage. Fig. 1(b) presents the common FRT grid codes (Lima et al., 2010). Considering the over and beneath the high and low voltage ride through border line, DFIG must be left out form the network via circuit breakers after authorized time of fault clearance.

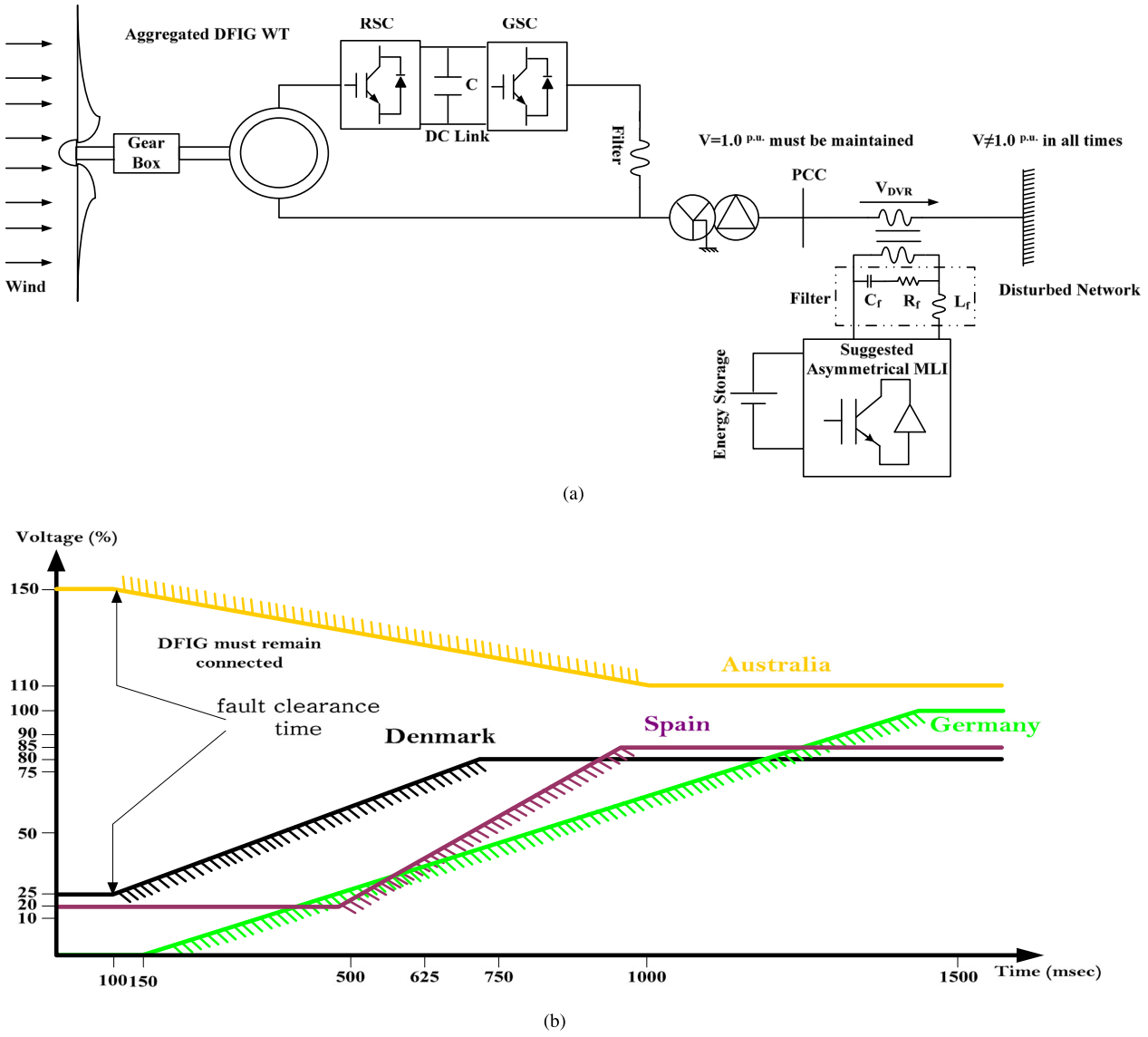

Fig. 1. (a) Single line diagram of power system, (b) different Fault Ride Through requirements of gird codes.

2.2. Mathematical model of DFIG

The pertinent relationships of the stator's voltages based on synchronous reference frame are explained as follows (Pena, 1996).

$$v_{ds} = R_s i_{ds} + \frac{d\lambda_{ds}}{dt} - \omega_e \lambda_{qs} \tag{1}$$

$$v_{qs} = R_s i_{qs} + \frac{d\lambda_{qs}}{dt} + \omega_e \lambda_{ds} \tag{2}$$

Also, relationships of the rotor's voltages based on synchronous reference are presented as follows:

$$v_{dr} = R_r i_{dr} + \frac{d\lambda_{dr}}{dt} - (\omega_e - \omega_r)\,\lambda_{qr} \tag{3}$$

$$v_{qr} = R_r i_{qr} + \frac{d\lambda_{qr}}{dt} + (\omega_e - \omega_r)\,\lambda_{dr} \tag{4}$$

where, λ_{dqr} and λ_{dqs} indicate d–q flux linkages of rotor and stator, respectively. v_{dqr} and v_{dqs} indicate d–q voltages of rotor and stator, respectively. i_{dqr} and i_{dqs} indicate d–q currents of rotor and stator, respectively. Also, ω_e indicate the electrical angular speed. The stator's fluxes in d–q frame can be presented as follows:

$$\lambda_{ds} = L_s i_{ds} + L_m i_{dr} \tag{5}$$

$$\lambda_{qs} = L_s i_{qs} + L_m i_{qr} \tag{6}$$

Also, the rotor's fluxes in d–q frame can be given by:

$$\lambda_{dr} = L_r i_{dr} + L_m i_{ds} \tag{7}$$

$$\lambda_{qr} = L_r i_{qs} + L_m i_{qs} \tag{8}$$

where, leakage inductance of rotor and stator are respectively represented by L_{lr} and L_{ls}, and also the resistances of rotor and stator are respectively represented R_r and R_s.

The active and reactive powers of stator are given by:

$$P_s = \frac{3.\left(v_{ds}.i_{ds} + v_{qs}.i_{qs}\right)}{2} = \frac{-3\left(L_m.L_s^{-1}.v_{qs}.i_{qr}\right)}{2} \tag{9}$$

$$Q_s = \frac{3\left(v_{qs}.i_{ds} - v_{ds}.i_{qs}\right)}{2} = \frac{3\left(L_m.L_s^{-1}.v_{qs}.\left(i_{ms} - i_{dr}\right)\right)}{2} \tag{10}$$

The *q-d* axis rotor current has controlled the active and reactive power of stator. Wind turbine has actually harvested a part of wind energy that it should be converted in the mechanical power (Betz, 1967; Hossain et al., 2010):

$$P_t = P_v C_P(\lambda, \beta_P) = 1/2\,\pi\,\rho R^2 C_P(\lambda, \beta_P)\,v^3 \tag{11}$$

$$C_P(\lambda, \beta_P) = c_1\left(\frac{c_2}{\lambda} - c_3\beta_P - c_4\right)e^{\frac{-c_5}{\lambda}} + c_6\lambda \tag{12}$$

3. Design and comparison of suggested asymmetrical MLI topology

By definition, the quality of provided voltage by AMLI is closely related to its created levels. A staircase sinusoidal voltage with high levels defines great voltage quality i.e., low THD. At best, it is required that number of switches to be increased that accordingly cost-price of inverter will be growth. In this paper, a novel AMLI is proposed which creates high-level staircase sinusoidal voltage with consideration of low switch number as compared to other popular and innovative AMLI structures. Overall structure of Suggested AMLI is presented in Fig. 2. As to Fig. 2, the suggested AMLI is configured based on Level Creator and H-bridge inverter that the values of DC sources have followed up special exponential form to create positive levels, then, the zero and negative levels have been created by H-bridge inverter.

In order to representing the working of suggested AMLI as to Fig. 2, the positions of all DC sources and switches have been defined by the subscripts and superscripts. Depending on the number of sub-MLIs i.e., DC sources and switches aimed to create required levels (e.g. 55 levels) marking of this subscripts and superscripts are easily figured out. In other words, subscribes' marks in each sub-MLI are determined based on number of DC sources in each sub-MLI, and also superscripts' marks are defined based on number of sub-MLIs.

However, the total number of utilized components in AMLI can be presented as follows:

$$N_{\text{Switch}} = n.(k+1) + 4 \tag{13}$$

$$N_{\text{DC,source}} = n \tag{14}$$

$$N_{\text{Capacitor}} = k.n \tag{15}$$

Where, N_{switch} and $N_{\text{DC,source}}$ respectively indicate total number of switches and DC sources. Also, n and k are respectively number of sub-MLIs and DC sources in each sub-MLI.

3.1. Operation of suggested AMLI

As stated by number of switches, the value of DC sources along with the relevant switching strategy the staircase sinusoidal voltage with required levels will be obtained. For better demonstrating the operation of suggested AMLI, definition of the of DC sources values and accordingly creating levels have been explained in detail as follows:

For sub-multilevel-1:

$$V_1 = V_{base} = k(k+1)^0 V_{DC} \tag{16}$$

For example, if number of sub-multilevel inverters is considered to be two units, then V_2^1 will be 1.

For sub-multilevel-2:

$$V_2 = k(k+1)^1.V_{DC} \tag{17}$$

Table 1
Different switching statuses of suggested AMLI with respect to $k = 2$ and $n = 3$.

ON switches	V_{out}	ON switches	V_{out}
$S_1^1, S_1^2, S_1^3, H_1, H_2$	1	$S_1^1, S_1^2, S_1^3, H_3, H_4$	−1
$S_2^1, S_1^2, S_1^3, H_1, H_2$	2	$S_2^1, S_1^2, S_1^3, H_3, H_4$	−2
$S_3^1, S_1^2, S_1^3, H_1, H_2$	3	$S_3^1, S_1^2, S_1^3, H_3, H_4$	−3
$S_1^1, S_2^2, S_1^3, H_1, H_2$	4	$S_1^1, S_2^2, S_1^3, H_3, H_4$	−4
	⋮		
$S_1^1, S_2^2, S_2^3, H_1, H_2$	13	$S_1^1, S_2^2, S_2^3, H_3, H_4$	−13
	⋮		
$S_2^1, S_3^2, S_3^3, H_1, H_2$	26	$S_2^1, S_3^2, S_3^3, H_3, H_4$	−26
$S_3^1, S_3^2, S_3^3, H_1, H_2$	27	$S_3^1, S_3^2, S_3^3, H_3, H_4$	−27
H_1, H_3	0^+	H_2, H_4	0^-

For another example, if three sub-multilevel inverters to be taken into account, taken V_2^2 will be 9.

For sub-multilevel-i:

$$V_i = k.(k+1)^{(i-1)}.V_{DC} \tag{18}$$

This exponential trend will be in the same way. As a consequence, maximum value of DC source will be:

$$V_n = k.(k+1)^{(n-1)}.V_{DC} \tag{19}$$

General Structure of Suggested Inverter:

When output voltage of sub-multilevel inverters to be summed, maximum value of output voltage will be:

$$V_{o,\max} = \sum_{i=1}^{n} V_{in,sub-multlvel,i} = \sum_{i=1}^{n}\left(k.(k+1)^{(i-1)} + 1\right).V_{DC} \tag{20}$$

Using H-bridge inverter, number of voltage levels can be presented as follows:

$$M_{\text{Level}} = \left(2.V_{o,\max}\right).V_{DC}^{-1} + 1 \tag{21}$$

However, the number of output voltage level is attained by:

$$M_{\text{Level}} = 2(k+1)^n + 1 \tag{22}$$

To verify and validate the working of this AMLI, its simplest model i.e., $n = 3$ and $k = 2$ is considered, however, 55-level $(2 * [2+1]^3 + 1 = 55)$ multilevel inverter is attained. Fig. 3(a–d) shows the output voltage of each sub-AMLI accompanying overall output voltage of AMLI. Meanwhile, different switching statuses related to providing staircase sinusoidal voltage by the AMLI are tabulated in Table 1.

3.2. Comparison of suggested AMLI with other popular and innovative asymmetrical topologies

To verify and validate the performance of the suggested AMLI, it has been compared with other popular and innovative asymmetrical topologies in terms of the number of voltage levels versus the number of utilized switches. In this regard, the most popular and innovative asymmetrical MLIs are considered as criteria to make a comparison with this structure. So, the relationships between number of utilized switches in the binary AMLI, trinary AMLI and innovative AMLI in: Babaei et al. (2014), Banaei et al. (2014), Farakhor et al. (2015) and Babaei et al. (2015) in terms of their created levels can be respectively presented as follows:

$$N_{\text{Switch,binary}} = 4\frac{\text{Ln}(M_{\text{Level}} + 1)}{\text{Ln}2} - 4 \tag{23}$$

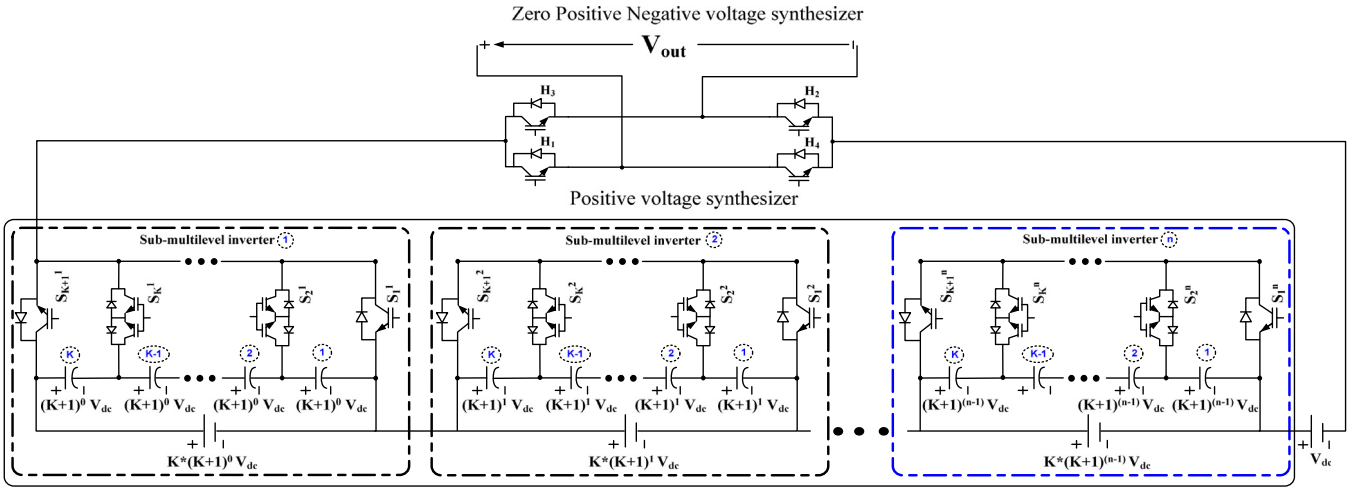

Fig. 2. Suggested asymmetrical multilevel inverter topology.

$$N_{\text{Switch,trinary}} = 4\frac{\text{Ln}(\text{M}_{\text{Level}})}{\text{Ln3}} \tag{24}$$

$$N_{\text{Switch,ref[37]}} = 4\frac{\text{Ln}(\text{M}_{\text{Level}}+1)-\text{Ln2}}{\text{Ln3}}+4 \tag{25}$$

$$N_{\text{Switch,ref[38]}} = 2\frac{\text{Ln}(\text{M}_{\text{Level}}+1)}{\text{Ln2}}+2 \tag{26}$$

$$N_{\text{Switch,[39]}} = 6\frac{\text{Ln}(\text{M}_{\text{Level}})}{\text{Ln5}} \tag{27}$$

$$N_{\text{Switch,[40]}} = \left[\text{Ln}\left(\frac{\text{M}_{\text{Level}}+1}{2}\right)\times\frac{3n-1}{\text{Ln}\,(n+1)}\right]+4 \tag{28}$$

As for Fig. 4, it can be certainly expressed that suggested AMLI creates high-level staircase sinusoidal voltage considering low number of switches as compared to the popular and innovative AMLIs.

4. Structure of BELBIC

BELBIC is based on the computational structure of the limbic system inspired by brain's emotional mechanism. It has imitated thalamus, amygdala, orbitofrontal cortex, sensory input cortex, and also further organs of brain which are responsible for the emotion procedure (Soreshjani et al., 2015b). BELBIC is constructed from two general divisions: regarding to the amygdala and orbitofrontal cortex. The amygdala's inputs are attained by the thalamus and cortical regions, as the orbital's inputs are attained by the cortical regions. Also, the system attains reinforcing (REW) signal. One *A* node exists for each stimulus *S* and one O node exists for each stimulant. Also, one output node exists in the same for the model output (MO). As the presented BELBIC structure in Fig. 5(a), MO node can be achieved by subtracting the outputs of *A* nodes and inhibitory outputs of *O* nodes i.e.,:

$$MO = \sum_i A_i - \sum_i O_i \tag{29}$$

Conversely, the inputs of Amygdala and Orbitofrontal Cortex do not project to the thalamic input. Eq. (30) states that emotional learning process has principally carried out in the Amygdala region:

$$\Delta G_{A_i} = \lambda.\left(S_i.\max\left(\left\langle REW - \sum_i A_i\right\rangle, 0\right)\right) \tag{30}$$

The learning principles related to the Orbitofrontal Cortex can be presented as follow:

$$\Delta G_{O_i} = \mu.S_i.R_o \tag{31}$$

where,

$$R_o = \begin{cases} \max\left(\left\langle \sum_i A_i - REW\right\rangle, 0\right) - \sum_i O_i & \forall REW \neq 0 \\ \max\left(\left\langle \sum_i A_i - \sum_i O_i\right\rangle, 0\right) & \forall REW = 0 \end{cases} \tag{32}$$

It is obvious that the orbitofrontal learning principles is same to the Amygdala principles. The orbitofrontal connection weight is just difference, which can increase or decrease as required to follow the essential inhibition. The following equations compute the nodes' values:

$$A_i = S_i.G_{A_i} \tag{33}$$

$$O_i = S_i.G_{O_i} \tag{34}$$

This system operates based on two levels: the amygdala portion learns to forecast and respond the designated reinforcer. Orbitofrontal system follows the discrepancies among the base system's forecasts and the definite designated reinforcer and learns for inhibition of the system output in accordance with the discrepancy. REW with respect to its entrance signals can be taken an objective function validation that is to say the reward and penalization have been utilized based on the previously determined objective function.

$$REW = f_{REW}\,(e, y, S_i)\,S_i.G_{O_i} \tag{35}$$

Likewise, the outputs of power plant and controller should be considered as the sensory inputs:

$$S_i = f_S\,(e, u, r, y) \tag{36}$$

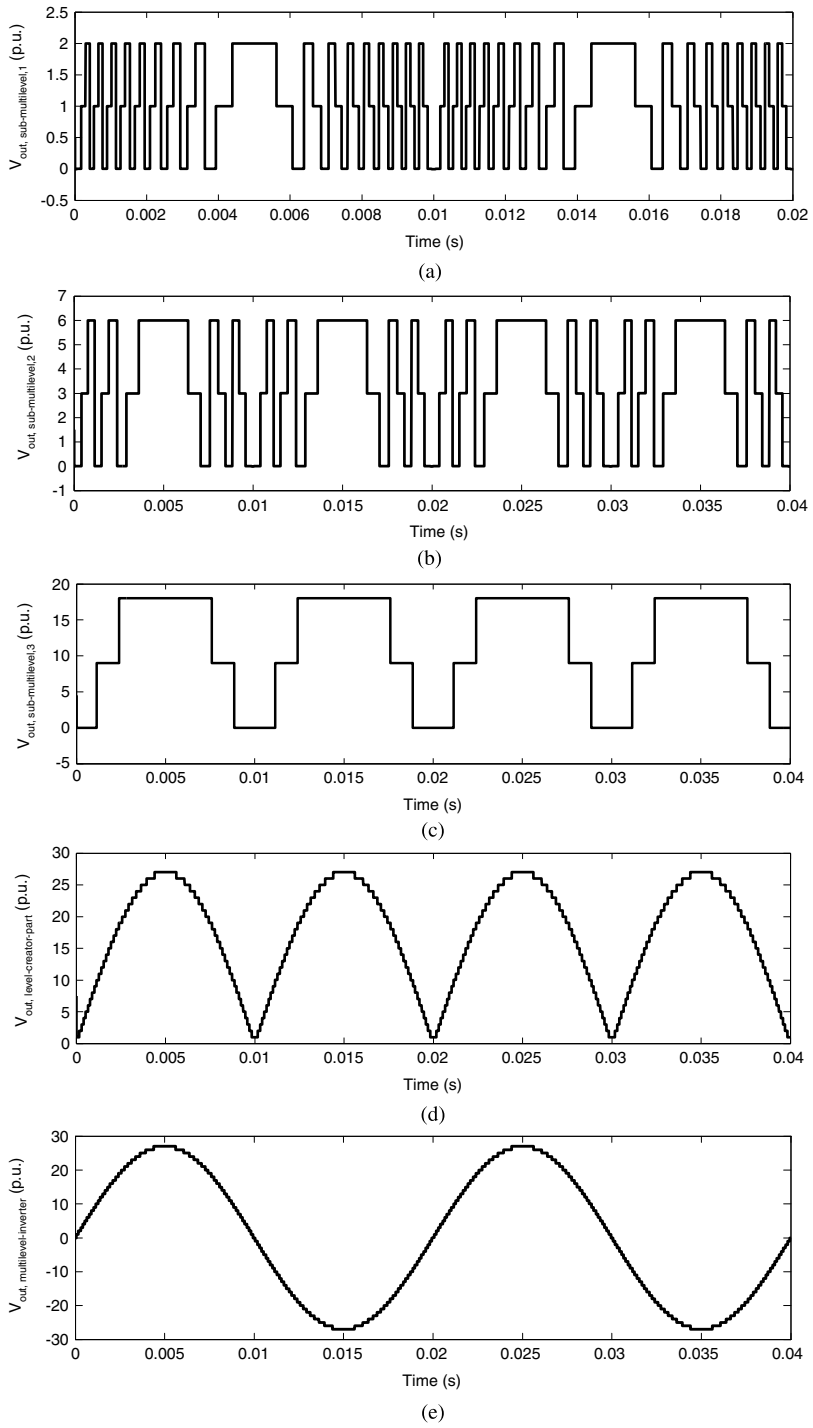

Fig. 3. (a) Output voltage of first sub-level creator, (b) output voltage of second sub-level creator, (c), (b) output voltage of third sub-level creator, (d), (b) output voltage of level creator, (e) output voltage of overall AMLI considering $k = 2$ and $n = 3$.

According to the aforementioned equations, sensory input and reward signal can be an optional function of r, u, e, and y. The construction of control system based on BELBIC is presented in Fig. 5(b). The relevant equations related to the reward signal and sensory input blocks can be presented as follows:

$$REW = \left(K_p + K_i.S^{-1} + K_d.S\right).e \tag{37}$$

$$S = K_s.e \tag{38}$$

Apart from effectual performance of BELBIC, its pertinent parameters must be optimally tuned so that the performance of this controller to be more increased. In this regard, this paper introduces the MOBA to optimally tune the BELBIC parameters. This algorithm will be explained in subsequence sections.

5. Design and construction of AMLI-BELBIC based DVR

5.1. Fault detection and compensation by DVR

Whenever a balanced or unbalanced voltage sag/swell or such-like occurs, the line's voltage is straightly measured and then transformed into d–q components based on Park and Clark transformations. Owing to probability of any fault occurrence in power

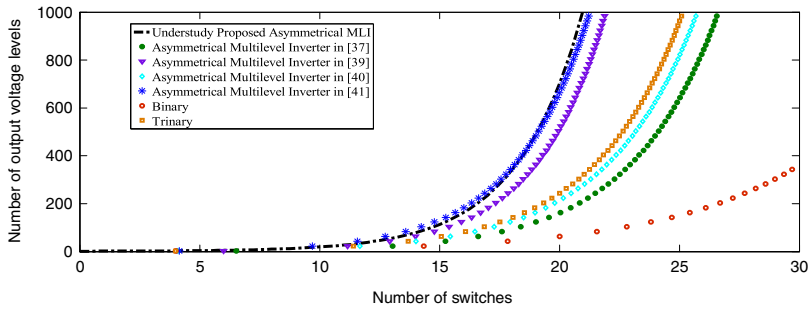

Fig. 4. Number of voltage levels versus number of switches in suggested inverter and other popular and innovative inverters.

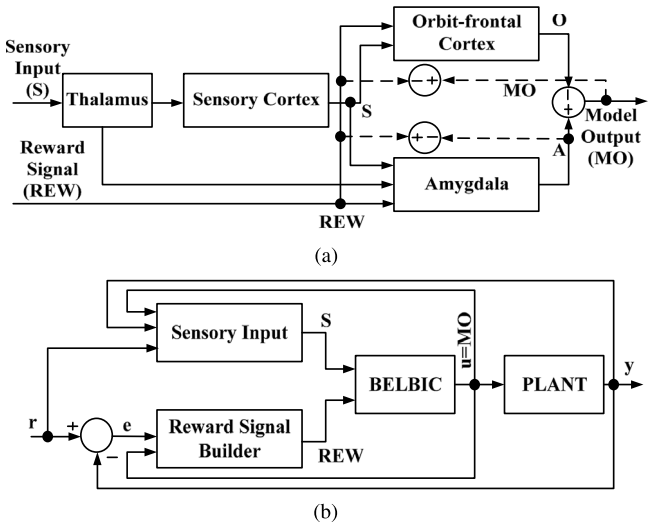

Fig. 5. (a) BELBIC structure, (b) BELBIC control system.

system, it must be taken three-phase input voltages of the PLL are unbalanced and harmonically contorted, i.e.:

$$V_{\mathrm{L,fa}}(t)=\sum_{n=1}^{+\infty}\left\langle V_n^+.\cos\left(n\omega t+\theta_n^+\right)+V_n^-.\cos\left(n\omega t+\theta_n^-\right)\right\rangle \tag{39}$$

$$V_{\mathrm{L,fb}}(t)=\sum_{n=1}^{+\infty}\left\langle V_n^+.\cos\left(n\omega t+\theta_n^+-2\pi/3\right)+V_n^-.\cos\left(n\omega t+\theta_n^--2\pi/3\right)\right\rangle \tag{40}$$

$$V_{\mathrm{L,fc}}(t)=\sum_{n=1}^{+\infty}\left\langle V_n^+.\cos\left(n\omega t+\theta_n^++2\pi/3\right)+V_n^-.\cos\left(n\omega t+\theta_n^-+2\pi/3\right)\right\rangle \tag{41}$$

θ_n^+/θ_n^- and V_n^+/V_n^- represent the phase and magnitude of the nth positive and negative sequence of the disturbed voltages. $V_{\mathrm{L,fa}}$, $V_{\mathrm{L,fb}}$ and $V_{\mathrm{L,fc}}$ are the sensed three-phase voltage at PCC or load position in the times of fault occurrence. The abc voltage is converted into the $\alpha\beta$ voltages using Clark transformation:

$$\begin{bmatrix}v_\alpha(t)\\ v_\beta(t)\end{bmatrix}=[T_{\alpha\beta}]\begin{bmatrix}V_{\mathrm{L,fa}}(t)\\ V_{\mathrm{L,fb}}(t)\\ V_{\mathrm{L,fc}}(t)\end{bmatrix}=\begin{bmatrix}v_\alpha^+(t)\\ v_\beta^+(t)\end{bmatrix}+\begin{bmatrix}v_\alpha^-(t)\\ v_\beta^-(t)\end{bmatrix} \tag{42}$$

where,

$$[T_{\alpha\beta}]=2/3\begin{bmatrix}1 & -1/2 & -1/2\\ 0 & \sqrt{3}/2 & -\sqrt{3}/2\end{bmatrix} \tag{43}$$

$$\begin{bmatrix}v_\alpha^+(t)\\ v_\beta^+(t)\end{bmatrix}=\begin{bmatrix}\sum_{n=1}^{+\infty}V_n^+.\cos\left(n\omega t+\theta_n^+\right)\\ \sum_{n=1}^{+\infty}V_n^+.\sin\left(n\omega t+\theta_n^+\right)\end{bmatrix} \tag{44}$$

$$\begin{bmatrix}v_\alpha^-(t)\\ v_\beta^-(t)\end{bmatrix}=\begin{bmatrix}\sum_{n=1}^{+\infty}V_n^-.\cos\left(n\omega t+\theta_n^-\right)\\ -\sum_{n=1}^{+\infty}V_n^-.\sin\left(n\omega t+\theta_n^-\right)\end{bmatrix} \tag{45}$$

Also, based on Park transformation $\alpha\beta$ voltages turned into d–q voltages:

$$\begin{bmatrix}v_d(t)\\ v_q(t)\end{bmatrix}=[T_{dq}].\begin{bmatrix}v_\alpha(t)\\ v_\beta(t)\end{bmatrix}=\begin{bmatrix}v_d^+(t)\\ v_q^+(t)\end{bmatrix}+\begin{bmatrix}v_d^-(t)\\ v_q^-(t)\end{bmatrix} \tag{46}$$

where,

$$[T_{dq}]=\begin{bmatrix}\cos(\theta) & \sin(\theta)\\ -\sin(\theta) & \cos(\theta)\end{bmatrix},\quad \theta=\omega t+\theta_1^+ \tag{47}$$

$$\begin{bmatrix}v_d^+(t)\\ v_q^+(t)\end{bmatrix}=\begin{bmatrix}\sum_{n=1}^{+\infty}V_n^+.\cos\left[(n-1)\omega t+\theta_n^+-\theta_1^+\right]\\ \sum_{n=1}^{+\infty}V_n^+.\sin\left[(n-1)\omega t+\theta_n^+-\theta_1^+\right]\end{bmatrix} \tag{48}$$

$$\begin{bmatrix}v_d^-(t)\\ v_q^-(t)\end{bmatrix}=\begin{bmatrix}\sum_{n=1}^{+\infty}V_n^-.\cos\left[(n+1)\omega t+\theta_n^-+\theta_1^+\right]\\ -\sum_{n=1}^{+\infty}V_n^-.\sin\left[(n+1)\omega t+\theta_n^-+\theta_1^+\right]\end{bmatrix} \tag{49}$$

But then, the measured faulty voltage can be presented as follows:

$$\begin{bmatrix}v_d(t)\\ v_q(t)\end{bmatrix}\cong\overbrace{\begin{bmatrix}\overline{v}_d\\ \overline{v}_q\end{bmatrix}}^{DC\ part}+\overbrace{\begin{bmatrix}\widetilde{v}_d(t)\\ \widetilde{v}_q(t)\end{bmatrix}}^{\text{Distortion part}} \tag{50}$$

$$\overline{v}_d=v_{d,1}^+\approx V_1^+ \tag{51}$$

$$\overline{v}_q=v_{q,1}^+\approx 0 \tag{52}$$

$$\widetilde{v}_d(t) = \sum_{n=2}^{+\infty} V_n^+ . \cos\left[(n-1)\omega t + \theta_n^+ - \theta_1^+\right] + \sum_{n=1}^{+\infty} V_n^- . \cos\left[(n+1)\omega t + \theta_n^- + \theta_1^+\right] \quad (53)$$

$$\widetilde{v}_q(t) = \sum_{n=2}^{+\infty} V_n^+ . \sin\left[(n-1)\omega t + \theta_n^+ - \theta_1^+\right] + \sum_{n=1}^{+\infty} V_n^- . \sin\left[(n+1)\omega t + \theta_n^- + \theta_1^+\right] \quad (54)$$

The faulty line voltage apart from type of contorted voltage has been heretofore figured out. From then, the required compensation voltage of DVR is calculated by:

$$e_{d,DVR}(t) = v_{d,p}(t) - v_d(t) \quad (55)$$

$$e_{q,DVR}(t) = v_{q,p}(t) - v_q(t) \quad (56)$$

Where, $V_{d,p}(t)$ and $V_{q,p}(t)$ are respectively the d–q voltages at pre-fault condition. As mentioned in previous section, the BELBIC-MOBA is here introduced to create accurate d–q reference signals of DVR. Furthermore, the results of BELBIC-MOBA have been thoroughly compared with PID-MOBA so that its performance to be more appeared, i.e.:

$$e_{d,DVR}{}^*(t) = K_{Pd}.e_{d,DVR}(t) + K_{Id}.\int_0^t e_{d,DVR}(t).dt + K_{Dd}.{}^{d}/_{dt}\, e_{d,DVR}(t) \quad (57)$$

$$e_{q,DVR}{}^*(t) = K_{Pq}.e_{q,DVR}(t) + K_{Iq}.\int_0^t e_{q,DVR}(t).dt + K_{Dq}.{}^{d}/_{dt}\, e_{q,DVR}(t) \quad (58)$$

The $\alpha\beta$ reference signals can be calculated based on Park's inverse transformation voltages:

$$\begin{bmatrix} e_{\alpha,DVR}{}^*(t) \\ e_{\beta,DVR}{}^*(t) \end{bmatrix} = \left[T_{dq}\right]^{-1} \begin{bmatrix} e_{d,DVR}{}^*(t) \\ e_{q,DVR}{}^*(t) \end{bmatrix} \quad (59)$$

The required three-phase reference signals based Park's inverse transformation can be calculated by:

$$\begin{bmatrix} e_{a,DVR}{}^*(t) \\ e_{b,DVR}{}^*(t) \\ e_{c,DVR}{}^*(t) \end{bmatrix} = \left[T_{\alpha\beta}\right]^{-1} \begin{bmatrix} e_{\alpha,DVR}{}^*(t) \\ e_{\beta,DVR}{}^*(t) \end{bmatrix} \quad (60)$$

The magnitude and phase angle of injected three-phase voltage by DVR is followed up as follows:

$$V_{DVR} = \sqrt{V_{Lp}^2 + V_{Lf}^2 - 2.V_{Lp}.V_{Lf}.\cos\left(\delta_{jump}\right)} \quad (61)$$

$$\theta_{DVR} = \tan^{-1}\left(\frac{V_{Lp}.\sin\left(\delta_{jump}\right)}{V_{Lp}.\cos\left(\delta_{jump}\right) - V_{Lf}}\right) \quad (62)$$

Where, V_{Lf}, V_{Lp} and δ_{jump} are respectively voltage after fault, voltage before fault and voltage's jumped phase due to fault occurrence.

5.2. Modulation to generate quasi-sinusoidal voltage by 55-level AMLI

There are some popular PWM approaches to perform modulation on MLI: IPD-PWM, POD-PWM, APOD-PWM, ST-PWM and PSC-PWM (Muthuselvi and Antony Samson, 2016). Among the Carrier Disposition PWM approaches; APOD-PWM introduces better performance as compared to others. In this paper, APOD-PWM strategy is used to generate the required pulses for 55-level AMLI switches' gates.

5.3. Multi-objective bees algorithm

This algorithm firstly developed by Prof. Duc Truong Pham and his college team at Cardiff University, that accordingly it has been implemented to solve the single objective problems (Pham et al., 2006). An upgraded version of BA has been constructed so that many non-dominated solutions to be identified. The multi objective problem is more unfathomable as compared to the single objective problem. These objectives interplay leads to an efficacious solutions set recognized as Pareto optimal solutions that create an optional determinative with more flexibility to extract a relevant alternative. The pseudo code of the BA in its basilar configuration for multi-objective optimization problems is presented in Fig. 6(a). Also, the mechanism of non-dominated MOBA approach is presented in Fig. 6(b).

The problem solution is mathematically introduced by:

$$f(X) = [f_1(X), f_2(X), \ldots, f_k(X)] \quad (63)$$

Subject to:

$$g_i(x) \le 0; i = 1, 2, \ldots, m \quad (64)$$

$$h_j(x) \le 0; j = 1, 2, \ldots, p \quad (65)$$

where $X = [X_1, X_2, \ldots, X_n]^T$ Which is decision variables' vector, f_i, $i = 1, 2, \ldots, k$ indicate the cost functions and g_i, h_j, $i = 1, 2, \ldots, m, j = 1, 2, \ldots, p$ indicate the problem's limitations.

For more perception of the Pareto approach, some determinations are presented as follows:

Determination 1. Crate two vectors $X, Y \in \Re^n$, is referred to $X \le Y$ if $x_i \le y_i$ for $i = 1, 2, \ldots, k$, and that X dominates Y (pointed to by $X \prec Y$) if $X \le Y$ and $X \ne Y$.

Determination 2. Expressed that a vector resolution variables $X \in \chi \subset \Re^n$ is non-dominated according to χ, provided no $X' \in \chi$ to the extent that $f(X') \prec f(X)$.

Determination 3. Expressed that a vector of resolution variables is Pareto optimal provided to be non-dominated according to F.

Determination 4. The Pareto Optimal Set P^* is defined as follows:

$$P^* = \{X \in F | X \text{ is Pareto optimal}\} \quad (66)$$

Determination 5. The Pareto Front PF^* is defined as follows:

$$PF^* = \left\{f(X) \in \Re^k | X \in P^*\right\} \quad (67)$$

Following adaptation procedure, parent and offspring will be merged to construct the population R_t (Chakraborty et al. 2009):

$$R_t = P_t \cup Q_t \text{ that } size(R_t) = 2N_P \quad (68)$$

A spectator bee deals with the nectar information thorough the recruited bees and engages a nectar sources according to the related probability with nectar source that can be presented as follows:

$$p_i = {}^{D_i}/_{N_P} \quad (69)$$

where, D_i is the solution number dominated by i solution. Here, spectator bee creates an adaptation on the position i.e., solution

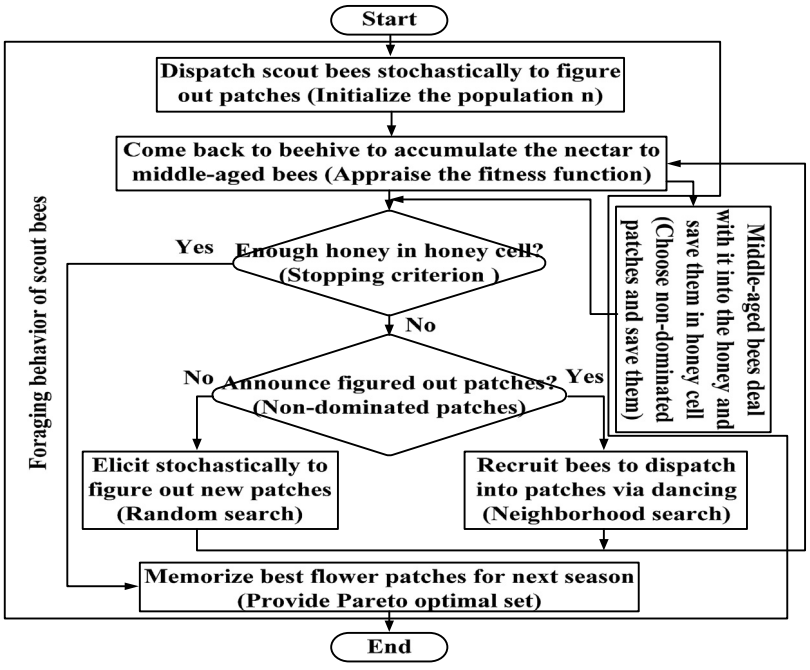

Fig. 6. (a) Pseudo code of the non-dominated MOBA, (b) mechanism of non-dominated MOBA approach.

in its mind and controls the nectar value of the nominated source i.e., solution:

$$X'_i = \left(x_{i0}, x_{i1}, x_{i2}, \ldots, x_{i(j-1)}.x'_{ij}.x_{i(j+1)}, \ldots, x_{i(D-1)}\right) \tag{70}$$

The value of x'_{ij} in X'_i solution can be also calculated by:

$$x'_{ij} = x_{ij} + u\left(x_{ij} - x_{kj}\right) \quad j \in [0, D-1],$$
$$k \in [0, N_P - 1],\ k \neq i,\ u \in [-1, 1]$$

5.4. Multi-objective problem formulation

Due to multi-objective nature of the problem resulted in momentousness of voltage quality; it is impressive that appropriate objective function to be formulated. In this regard, to augment the quality of injected voltage by *AMLI-BELBIC based DVR* two prominent issues are presented as follows:

$$\text{Minimize } F_1 = \int_{t=0}^{t=t_{sim}} \left(\Delta e_{d,DVR}(t)\right).t.dt \tag{71}$$

$$\text{Minimize } F_2 = \int_{t=0}^{t=t_{sim}} \left(\Delta e_{q,DVR}(t)\right).t.dt \tag{72}$$

6. Results and discussions

To verify and validate the performance of suggested DVR in order to augment the FRT capability of DFIG, different types of balanced and unbalanced voltage sags and swells occur in the power system. As mentioned before, the multi-objective optimization problem is performed both the BELBIC and PID. Optimal parameters of both the controllers are presented in Tables 2 and 3. Moreover, Fig. 7 portrays the Pareto front resulted from MOBA.

6.1. Deep, ramp, shallow and unbalanced voltage sags

To enhance the FRT capability of DFIG, *AMLI-BELBIC based DVR* has been accurately and thoroughly assessed under different kinds of voltage sags. So, it is considered that the power system to be seriously affected by a 100% voltage sag at $t = 0.05$ s that is cleared 100 ms later, then the disturbed voltage has gradually gone to the 80% original voltage and persists for 100 ms. Then, an unbalanced voltage sag happens at $t = 0.35$ s with 100 ms duration that is cleared after 100 ms, and subsequently the PCC voltage returns into its nominal condition. Therefore, the disturbance is at once detected to indwell the suggested DVR aimed for injection of the

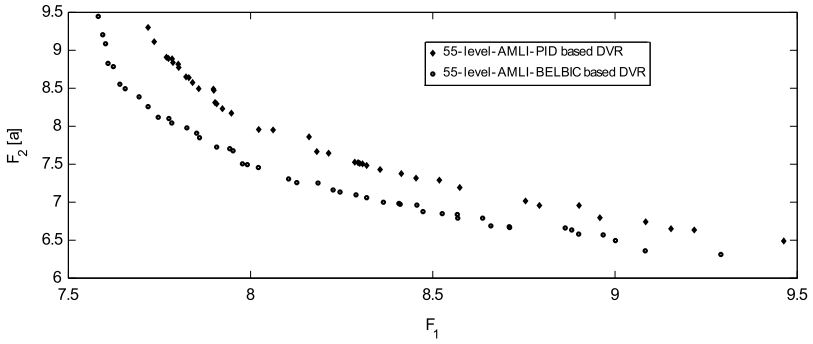

Fig. 7. Pareto optimization front resulted from MOBA.

Table 2
Optimal BELBIC parameters of AMLI-BELBIC based DVR.

K_{Pd}	K_{Id}	K_{Dd}	K_{Sd}	λ_d	μ_d	K_{Pq}	K_{Iq}	K_{Dq}	K_{Sd}	λ_q	μ_q
23.025	4.703	1.191	19.46	0.003	0.007	14.901	3.046	1.38	13.38	0.002	0.005

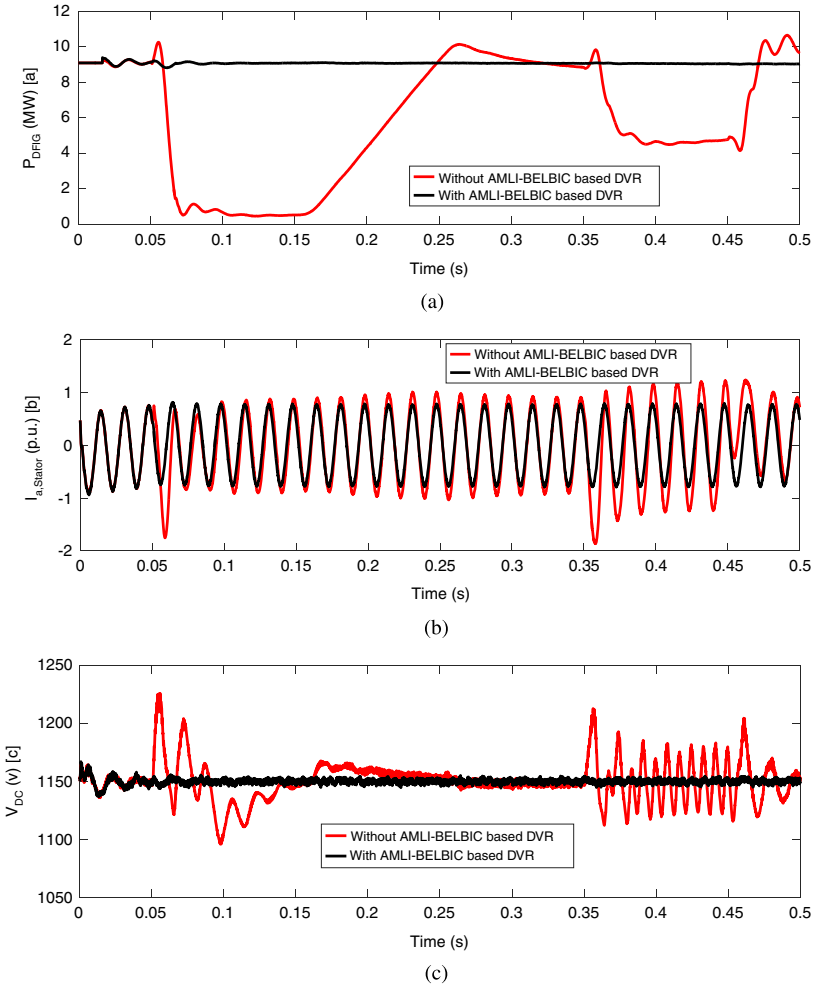

Fig. 8. (a) Active power of DFIG (c) Stator current of DFIG (d) DC-link voltage of DFIG.

required three-phase voltage so that the voltage at PCC to be retrieved into the pre-disturbance status. However, the simulation results are presented in Fig. 8(a–c). These figures have essentially proved that the suggested DVR has significantly enhanced the FRT capability of DFIG. Furthermore, the simulation results for *AMLI based DVR* based on PID-MOBA and BELBIC-MOBA are respectively presented in Fig. 9(a–d) and Fig. 10(a–d) that they have definitely confirmed the effectiveness of *AMLI-BELBIC based DVR* to accurately

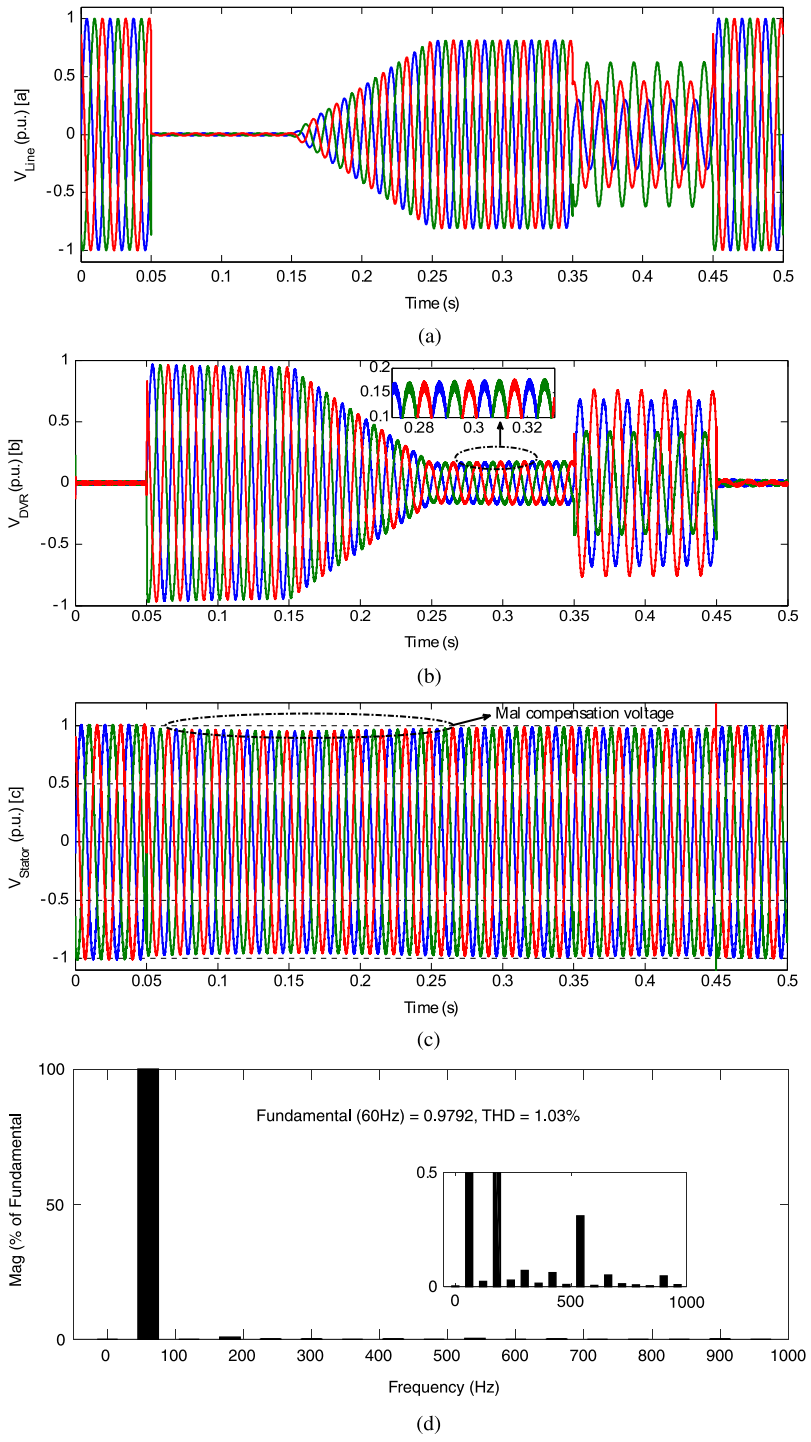

Fig. 9. (a) Disturbed network voltage, (b) injected voltage by AMLI-PID based DVR, (c) stator voltage of DFIG with AMLI-PID based DVR, (d) FFT of compensated voltage by AMLI-PID based DVR.

compensate different voltage sags i.e., augment both power quality and FRT capability of DFIG.

6.2. Severe, ramp, slight and unbanned voltage swells

Voltage swell is often occurred due to the sudden throwing off the several inductive loads or energizing a great capacitor bank. Depending on the amount of these inductive loads, severe or slight voltage swell may be revealed. It is worth mentioning that, DVR is the main responsible for compensating this most likely incident. In this regard, different types of voltage swells are here considered so that the performance of *AMLI-BELBIC based DVR* to enhance the FRT capability of DFIG to be evaluated. Hence, the power system is seriously affected by a 100% voltage swell at $t = 0.05$ s that is cleared 100 ms later, subsequently the disturbed voltage has gradually gone to the 120% original voltage and persists for 100 ms. Then, an unbalanced voltage swell happens at $t = 0.35$ s with 100 ms duration that is cleared after 100 ms, and afterward the PCC voltage returns into its nominal state. As soon as detecting the disturbance, the suggested DVR injects the required three-phase

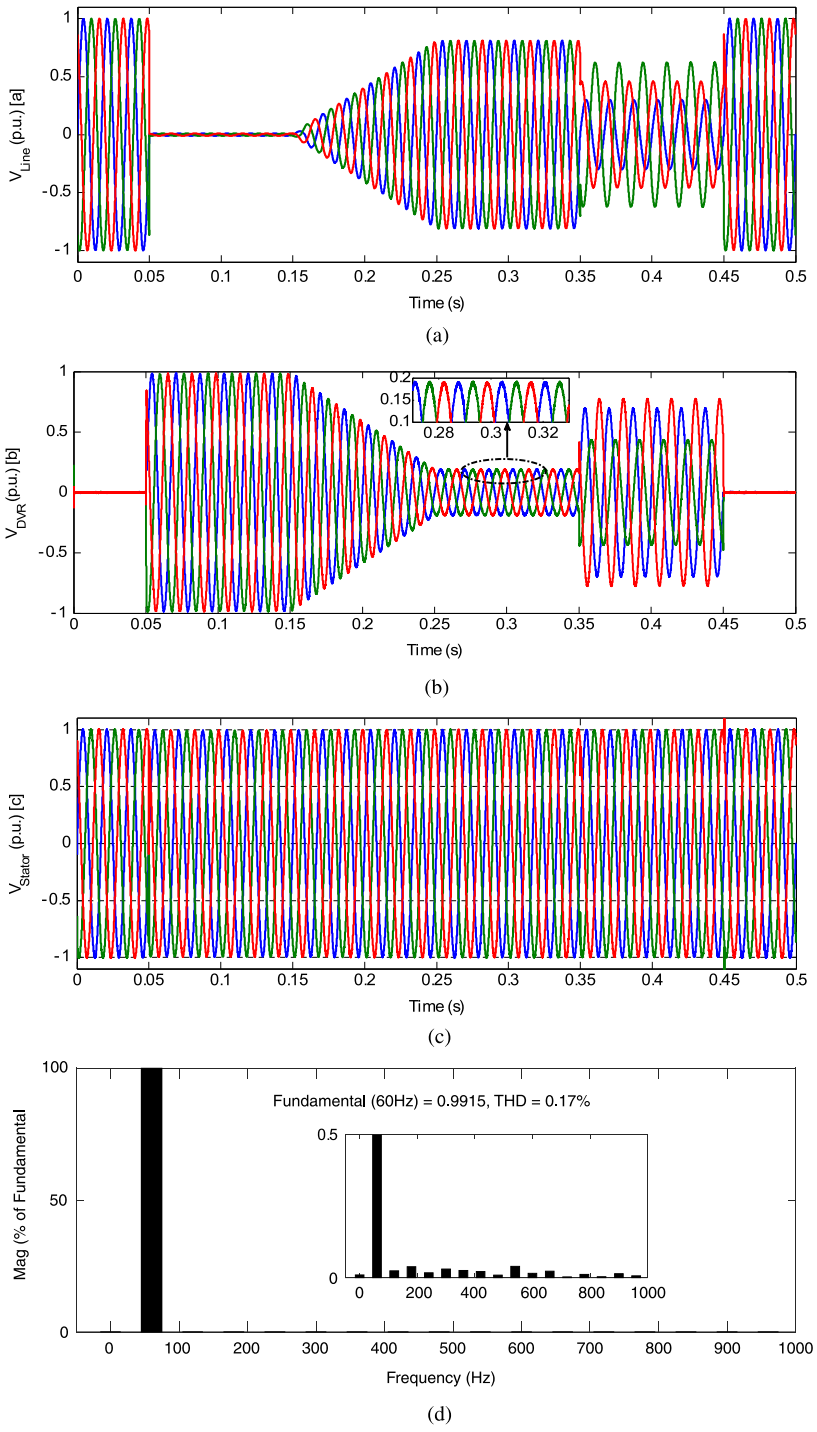

Fig. 10. (a) Disturbed network voltage, (b) injected voltage by AMLI-BELBIC based DVR, (c) stator voltage of DFIG with AMLI-BELBIC based DVR, (d) FFT of compensated voltage by AMLI-BELBIC based DVR.

voltage so that the PCC voltage to be brought back into the pre-disturbance state. As expected and according to the simulation results presented in Fig. 11(a–d) and Fig. 12(a–d), the performance of *AMLI-BELBIC based DVR* has certainly validated to accurately compensate different voltage swells i.e., augment both power quality and FRT capability of DFIG.

Table 3
Optimal PID parameters of AMLI PID based DVR.

K_{Pd}	K_{Id}	K_{Dd}	K_{Pq}	K_{Iq}	K_{Dq}
26.44	3.98	1.29	20.67	2.36	1.19

7. Conclusion

In this paper, a new AMLI structure based on upside-down form of DC sources is primarily introduced so that high level staircase sinusoidal voltage with respect to low switch number to be created. Effectual performance of suggested AMLI has been compared with other popular and innovative asymmetrical struc-

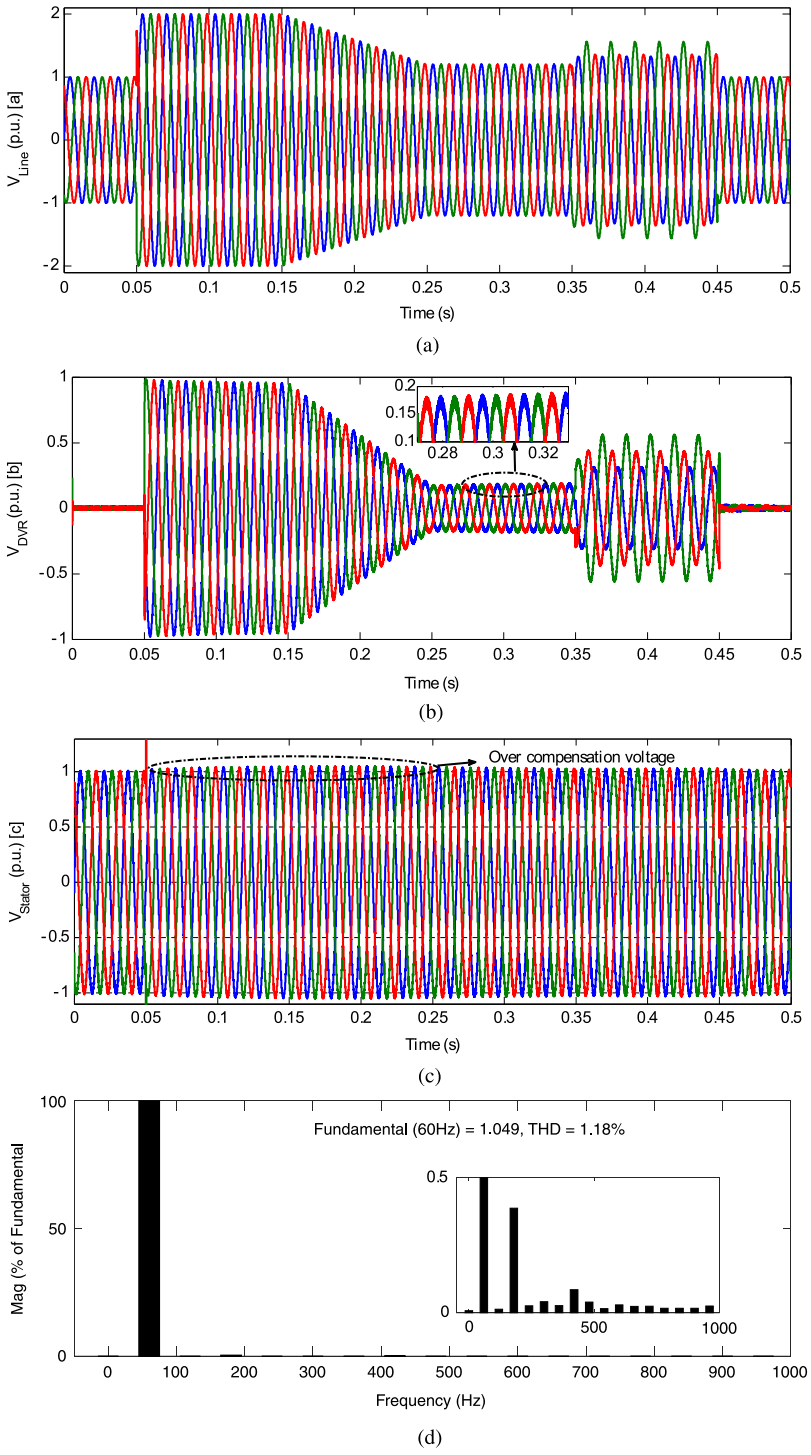

Fig. 11. (a) Disturbed network voltage, (b) injected voltage by AMLI-PID based DVR, (c) stator voltage of DFIG with AMLI-PID based DVR, (d) FFT of compensated voltage by AMLI-PID based DVR.

tures in terms of the number of created levels versus the number of utilized switches. The suggested AMLI is indwelt in the DVR to compensate different severe/slight balanced/unbalanced voltage sags and swells with the aim of augmentation of DFIG's FRT capability. To better regulate the references signals of *AMLI-BELBIC based DVR*, BELBIC controller is settled in DVR's system control. Likewise, in view of the multi-objective nature of the problem, MOBA is employed to optimally tune the parameters of both the BELBIC and PID controllers so that the power quality problem to be more assessed. On the whole, the relevant analytical studies along with the simulation results have essentially certified the performance of suggested AMLI as compared to other popular and innovative AMLIs. Also, *AMLI-BELBIC based DVR* has accordingly compensated different severe/slight balanced/unbalanced voltage sags and swells so that DFIG can follow its normal operation.

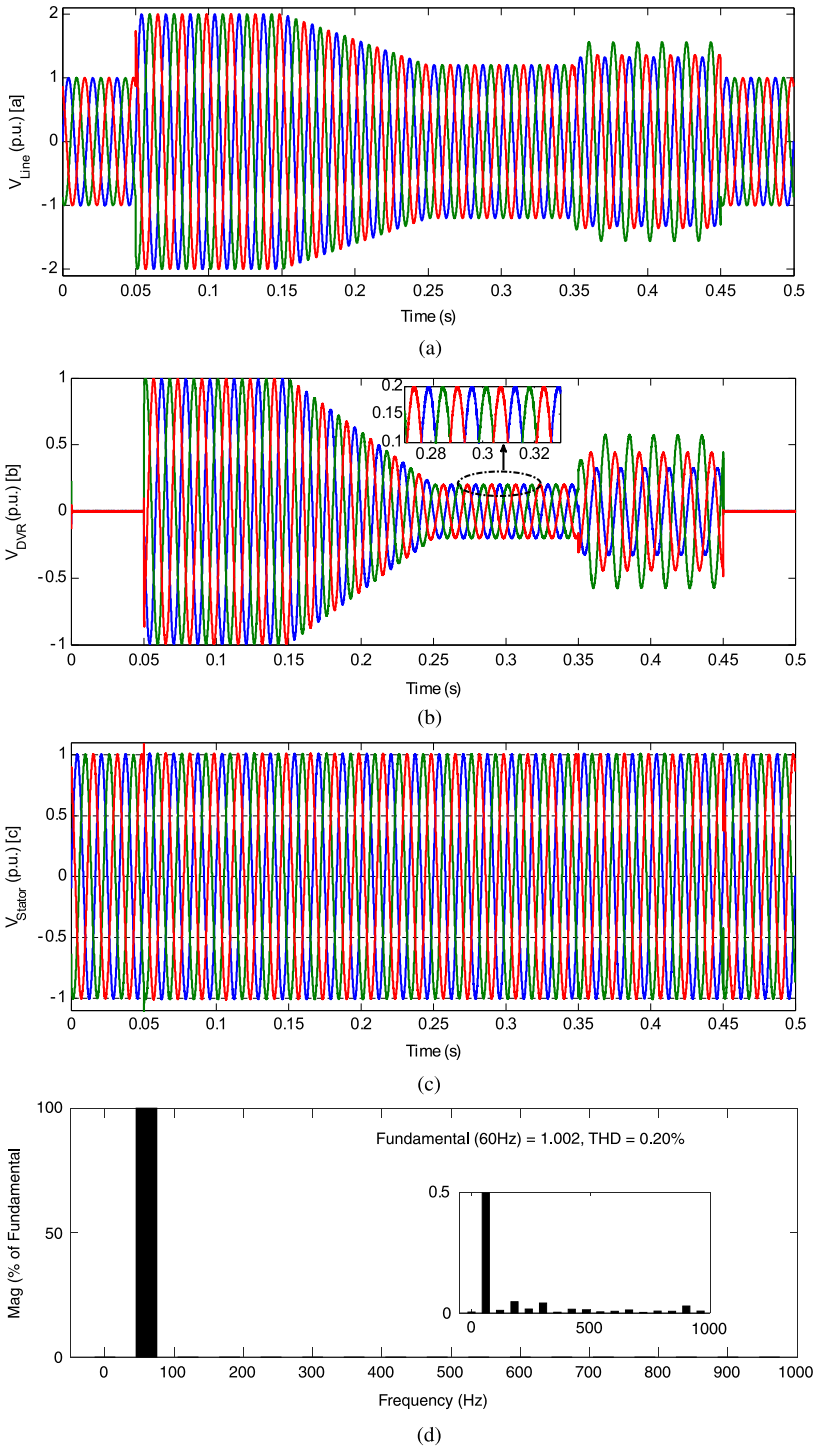

Fig. 12. (a) Disturbed network voltage, (b) Injected voltage by AMLI-BELBIC based DVR, (c) stator voltage of DFIG with AMLI-BELBIC based DVR, (d) FFT of compensated voltage by AMLI-BELBIC based DVR.

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