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# A comparative analysis of the location behaviour of the global semiconductor manufacturers

Tomokazu Arita\* and Philip McCann\*\*

## **Abstract**

In this paper, we explain the structure and technological relationships between the different sub-sectors of the global semiconductor industry, by analyzing firm-level micro data including production technological indices of wafer manufacturing processes and firm-alliances. Our results indicate that the economic geography and the location behavior of the global semiconductor industry are diverse and also fundamentally different to the types of location behavior commonly accepted in the past academic arena.

## ***1. Introduction***

Much of the current literature on hi-tech developments within the electronics industry tends to focus on the spatial and organisational arrangements evident in innovative clusters such as Silicon Valley. There are, however, many very different forms of spatial organisation which engender innovations within the semiconductor industry, and these variations depend on the particular sub-sector of the semiconductor industry. In this paper we discuss the case of US, European and Asian semiconductor producers. The paper will analyse data from over 100 semiconductor plants operated by over 50 firms located within the US, Europe and Asia. In particular, we will focus on the firms undertaking the wafer manufacturing processes. As we will see in this paper, in order to discuss the geographical behaviour of many parts of the semiconductor industry, it is necessary to consider not only organizational issues, but also the different sub-sectors within the industry. From these perspectives, many of the generalizations made about the semiconductor industry based on observations of Silicon Valley are seen to be rather inappropriate.

This paper is organized as follows. In section 2 we review the types of arguments frequently associated with discussions about the spatial organization of the semiconductor industry and spatial patterns of innovation. In section 3, we describe in detail the structure and organization and activities which take place within the semiconductor industry, and in particular we focus on the three different components of the semiconductor industry. As we will see, many of the issues raised in section 2 really only relate to one sub-sector of the electronics industry, and the two other parts of the industry have been almost entirely ignored in the literature. In section 4 we discuss our methodological approach, which involves using cluster analysis to group semiconductor plants according to their technological trajectories and activities, and this is done by using detailed indices of product innovations within the wafer-processing sub-sector of the industry. We then use this information to construct diagrammatic representations of the spatial and technological structure of the global industry in each of the three super-regions of the USA, EU and Asia over the period 1995 to 2004. This allows us to observe

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trends in the spatial and technological structure of the global industry over this period. This exercise is then also repeated in the case of four individual global semiconductor producers, in order to help us identify how these global changes are manifesting themselves at the level of the individual corporate firm. We find very little support for a simple product-cycle type explanation of these global changes. In order to account for these findings, in section 5 we therefore explore the organizational issues governing the spatial patterns of product innovations within the semiconductor industry.

## ***2. Geography and the semiconductor industry***

Over the last decade there has been a significant growth in interest in the geographical behaviour of firms in the electronics and semiconductor industry (Oahey and Cooper 1989; Saxenian 1994; Almeida and Kogut 1997; Kittiprapas and McCann 1999). There are a variety of interrelated reasons for this recent research interest, which can broadly be grouped into three themes. The first theme is a general renewal of academic interest in geography and industrial location issues per se. This has been encouraged in part by the continuing process of economic integration in many parts of the world, such as the EU, NAFTA, ASEAN and MERCOSUR, as well as by the writings of certain influential commentators (Porter 1990; Krugman 1991). The second theme is a growth in interest in the particular characteristics of the electronics and semiconductor industry itself. The reason for this is partly that electronics industry, and in particular the semiconductor part of the electronics industry, is generally regarded as an industry which is both highly successful, and also at the forefront of human technological development (Piore and Sabel 1984; Best 1990). While individual consumer electronics sub-sectors within the electronics industry are highly cyclical, the semiconductor and microchip production industry is rather less volatile than household or consumer electronics sectors, because this sector provides the basic technological developments and inputs for all of these other imperfectly correlated consumer electronics sectors. At the same time, innovations in this semiconductor industry are often embodied into the production technology of other non-electronics industries, thereby generating induced productivity effects. Therefore, on account of this process of the onward transmission and embodiment of new technologies from the semiconductor industry into other electronics and non-electronics industries, it is implicitly assumed by many commentators that observation of the behaviour of the electronics and semiconductor sector may also provide clues as to the future technological trajectory of other industrial sectors in general. A third reason for the growth in interest in the electronics and semiconductor industry has been the apparent tendency of this industry to cluster in particular locations such as Silicon Valley (Scott 1988, 1991; Saxenian.1994; Angel 1991). The result of this behaviour is that certain areas appear to exhibit high growth performance in this sector, while other areas have been unable to develop any equivalent industry base (*The Economist* 1997). This has led to concern among public policy planners in various countries and regions (Castells and Hall 1994) to understand the economic-environmental conditions under which such industrial clusters are fostered, in the hope of replicating these conditions elsewhere.

In order to generate such an array of new product developments, these combined features are assumed to imply that the semiconductor industry will also tend to be at the

forefront of organizational developments (Eisenhardt and Schoonhoven 1990) and production process innovations (McCann and Fingleton 1996). Therefore, observation of the current organizational behaviour of the semiconductor industry may point towards the future behaviour of industry in general, as other industrial sectors attempt to imitate the successful organization and production innovations exhibited by this sector. Indeed, much of the current thinking about the optimal relationship between industry organization and geography has been developed on the basis of observations of the large numbers of small and medium sized semiconductor firms in locations such as Silicon Valley (Saxenian 1994; Scott 1988, 1991; Larsen and Rogers 1984). In many circles (Keeble and Wilkinson 1998) it has now become almost a matter of faith that many small and medium sized firms clustered at the same location will guarantee the maximum levels of product innovation (Aydalot and Keeble 1988; Saxenian 1994). The logic behind this argument is that such small firms are assumed to find it not only relatively easy to share information and to benefit from local information spillovers, but also to reconfigure their organizational and input-output linkages appropriately as new product developments occur. Empirical support for these arguments, which appears to confirm the local presence of industry-specific informal information spillovers, comes primarily from patent citation counts (Jaffe et al. 1993; Almeida and Kogut 1997). Meanwhile, these observations of the high growth performance of small firm clusters such as Silicon Valley (Saxenian 1994), Cambridge UK (Castells and Hall 1994) and Ile de France (Scott 1988) are contrasted with the relatively weaker growth performance of the large-firm parts of the electronics industry (Saxenian 1994). Explanations for the apparent difference in the growth performance of the small and large firm sectors are based on the assumptions that the organizational rigidity and well-defined boundaries of large hierarchical firms, limit the ability of large firms to respond appropriately to the rapid market changes of these new industries (Saxenian 1994). Small firm clusters are therefore perceived to represent the future optimal spatial and organizational arrangements in industries with very short product life cycles (Piore and Sabel 1984; Porter 1990; Saxenian 1994).

Such arguments, however, are based on very strong assumptions about the relationship between information generation, knowledge exchanges and geographical scales. Following Marshall (1920) and Vernon (1960), this clustering argument is based on the assumption that knowledge spillovers are generated and realised specifically at the geographical scale of the local urban area. Urban clustering is therefore assumed to be advantageous for industries which exhibit very short product life-cycles (Vernon 1966, 1979). Yet, recent research within the electronics and semiconductor industry (Suarez-Villa and Rama 1996; Suarez-Villa and Karlsson 1996; Wever and Stam 1988) suggests that agglomeration linkages, and the formal outcomes of any informal knowledge spillovers (Audretsch and Feldman 1996; Suarez-Villa and Walrod 1997; Arita and McCann 2000), extend over much larger spatial scales than that of the individual urban metropolitan area. In the case of multi-plant multinational firms (Cantwell and Iammarino 2000), any such agglomeration effects may even operate over spatial scales larger than individual countries. These empirical observations therefore cast doubt on the assumed importance of specifically local inter-firm knowledge spillovers as a source of competitive advantage (Porter 1990, 1998) within the electronics industry, and point

rather more to the role of labour market hysteresis as a possible rationale for industrial clustering (Angel 1991; Arita and McCann 2000). More importantly, however, these observations also cast doubt on the whole hypothesis that small firm clusters represent something of an ideal spatial and organizational arrangement ensuring the maximization of innovation, either for the semiconductor industry or any other innovative industry facing short product life-cycles. Moreover, the fact that among the large-firm sectors there are winners and losers, suggests that similar arguments also holds for large firms. Without detailed industry and firm-level information regarding the relationship between firm innovation, entrepreneurship, and decision-making structures and processes, we must be cautious about over-generalising about the optimal structure, organizational and geographical behaviour of the industry.

Part of the problem here is that so much of the literature which purports to show a high correlation between spatial industrial clustering, small and medium sized firms and short product life-cycles, has tended to focus on the spatial and organizational issues of only one particular part of the global electronics and semiconductor industry. The electronics industry as a whole is comprised of many sub-sectors ranging from the semiconductor industry to the consumer electronics sectors, and the semiconductor industry itself is comprised of three quite distinct sub-sectors, defined in terms of the nature of the activities and the transactions they undertake. Observations of Silicon Valley and the 'Cambridge Phenomenon' (Castells and Hall 1994) are actually primarily observations of groups of small firms whose activities correspond solely to only one of the three sub-sectors within the semiconductor industry, namely the Design sector. Yet, there are also many large vertically-integrated firms in this same sub-sector of the industry which are almost entirely ignored by the literature. Similarly, the other two parts of the semiconductor industry, the Wafer Process and the Wafer Manufacturing sectors, are characterized almost entirely by vertically-integrated wafer manufacturing and assembly firms. The spatial and organizational arrangements of the vertically-integrated parts of the semiconductor are completely different to the small semiconductor firms (Arita and McCann 2002a,b,c, 2004, 2006; McCann et al. 2002). The relationships between geography and technology within the semiconductor must therefore be considered individually for each of the three sub-sectors of the industry. Only in this way can we assess whether or not the types of spatial and organizational arrangements of Silicon Valley are more generally applicable to the parts of the industry.

Firm location behaviour within the semiconductor industry is often the result of different, and sometimes rather conflicting, objectives. Rarely is the geographical result in reality a Silicon Valley-style spatial clustering of highly innovative small firms generating very short product life-cycle outputs. The fact that this is a rare phenomenon is partly why such high-technology clusters are of interest, but also it is why generalizations based on such observations should be avoided. In order to appreciate these points we must first discuss the nature and organization of the semiconductor industry itself.

### ***3. The Organization of the Semiconductor Industry***

In order to understand the organization of the semiconductor industry it is first necessary to understand the different activities which take place within the industry (Nishimura 1995, 1999). As we see in Fig.1, the different activities in the semiconductor industry can be compared more or less directly with the different activities which take place in the book publishing industry.

The first stage of the production process is the silicon chip design stage, in which the functional logic of the microchip, and three-dimensional circuit layout of transistors and capacitors within the silicon wafer is determined. This activity is carried out primarily using computer aided design (CAD) systems. This stage of the process can be compared with the planning, editing and layout stages of the book publishing process. The result of this stage is the production of masks, which are the three-dimensional templates of the chip. These Integrated Circuit (IC) design activities are undertaken both by the large number of small specialized IC design firms, and also by large vertically-integrated semiconductor producing firms. The activities are provided for by specialist CAD vendor firms which provide customized design software for the designers. At the same time, there has also emerged recently a sub-sector of the industry which is concerned only with the construction of intellectual property rights relating to IC designs. These firms design only logic functions without circuit layouts, and act in consultation with both small and large IC design firms in order to ensure patents are granted for the new chip protocol designs. The number of firms involved in this stage of the production process has grown enormously during the last two decades, with small design-oriented firms tending to be clustered in locations such as Silicon Valley. It is this part of the industry which has received so much academic attention. Yet, there are still very many IC design activities which take place within vertically-integrated semiconductor producers both inside and outside of Silicon Valley, with locations in other parts of the USA, as well as both Europe and Asia. These are the types of firms which we will investigate in this paper with our examples here being Intel, Texas Instruments, Philips and Toshiba. Other such firms are NEC, Mitsubishi (Arita and McCann 2000a), Sanyo, OKI, Motorola (Arita and McCann 2004), Sony, Sharp, Rohm (Arita and McCann 2002c), Fujitsu, NEC, OKI, Rohm (Arita and McCann 2002b), Matsushita and Hitachi (Arita and McCann 2006).

The second stage of the process is the wafer process, the technology of which is determined by materials science. At this stage of the production process the circular silicon wafers, produced by specialist chemicals firms, are subjected to lithography. This is a process whereby ultra-violet light is used to illuminate certain parts of the wafer, according to the mask design, in order to bring about chemical changes within certain parts of the wafer. The wafers are then etched and treated, thereby removing the parts of the wafer subjected to the lithography. After as many as fifteen stages of lithography and treating, the result is a three-dimensional silicon structure. This stage of the semiconductor production process can be compared to the plate-making and phototype process which takes place in the book printing industry.

The final stage of the wafer production process is that of the wafer assembly process. Here, the circular wafers which have been subjected to lithography and treating are extracted and dissected into many small square chips, each of which is then framed in

plastic or ceramics for insulation and protection. This stage of the chip production process is the equivalent of the book binding process within the book publishing industry. The level of technology of the second and third stages of the wafer and assembly process is defined in terms of the minimum processing rule and the wafer size. The minimum processing rule is the definition of the level of miniaturization of the technology, and the wafer size is the size of the individual silicon wafers which can be produced and then dissected to produce chips. The smaller is the minimum processing rule and the greater is the wafer size, the more advanced is the technological generation. In terms of technology, the second and third stages of the semiconductor production process are just as important to the semiconductor industry as the first stage, and the product life-cycles are just as short. Different minimum processing rules and wafer sizes represent completely different generations of technology.

The majority of these second and third stage activities tend to be carried out by two groups of firms in more geographically dispersed locations outside of the US (Arita and McCann 2002a,b,c; 2006), and this may explain why these sectors have received relatively little academic interest. The first group of firms undertaking the wafer and assembly processes are the vertically-integrated semiconductor producers such as Intel and NEC, which undertake all of their own chip design and manufacturing activities. Firms such as NEC (Nippon Electronics Company), Philips, Fujitsu and Motorola, which also manufacture finished goods, produce for internal demand as well as for other consumer firms, whereas firms such as Intel produce entirely for external customers. The common feature of the production of these firms is high volumes. The second group of firms undertaking the wafer and assembly processes are the specialist East Asian sub-contracting IC manufacturing firms. These are primarily Taiwanese (*Business Week* 2005), Korean and Japanese firms. They are comprised of a small number of specialist large firms, such as the Taiwan Semiconductor Manufacturing Company, which have both the capacity to produce ICs in large numbers, and also the technology to allow both the high degree production specificity and flexibility required to manufacture custom-designed ICs. The second and third stages of the semiconductor manufacturing process are at least as technologically advanced as the first stage, requiring enormous physical, financial and human capital inputs. Therefore, simple observations based primarily on contrasts between Silicon Valley and other parts of the semiconductor industry (Saxenian 1994) are of very limited analytical use for more general industry-organization discussions.

Having discussed the nature of the semiconductor industry, in the next section we will look at the relationship between technological change and spatial industrial organization in the case of the semiconductor manufacturers who are located in the US and Europe. In particular we will focus on those firms which carry out the second and third-stage wafer process and assembly activities. The object of this exercise is to assess the extent to which orthodox product life-cycle approaches can broadly account for the technology-space relationship.

#### ***4. Data and Analysis***

The data we employ comes from the Strategic Marketing Association: ED Research (1995, 2004) compendium of the semiconductor industry, and provides individual production line data for every semiconductor firm located within the US, Europe and Asia for 1995 and 2004. The total number of such firms and production lines, in terms of the equivalent number of 6 inch (150mm) wafers produced in each region are described in the Table 1.

Table 1

	US	EU	ASIA	JAPAN	Rest of ASIA
1995					
Total Firms	153	56	144	47	100
Total production lines	353	119	439	276	163
Production Fab	193	99	344	211	133
R&D-Pilot	160	20	95	65	30
Total Production Capacities	2,855,137	1,447,853	5,969,949	3,950,919	2,019,030
2004					
Total Firms	110	66	153	67	88
Total production lines	198	123	445	277	168
Production Fab	118	98	349	220	129
R&D-Pilot	80	25	96	57	42
Total Production Capacities	3,531,655	2,509,293	10,737,574	4,575,497	6,162,078
Total Production Capacities(6 inch wafers:equivalent)					

In terms of general establishment data, SMA-EDR compendium provides us with the location details of each plant. For technology indices, the SMA-EDR provides us with information on the minimum processing rule and the wafer size of the products produced at each location. In the case of the minimum processing rule, a smaller size represents a newer vintage of technology, whereas in the case of the wafer size, a larger size represents a newer technology. SMA-EDR also provide us with details of the wafer processing capacity, of the plant in terms of the total number of silicon wafers produced annually. As far as we are aware, such detailed semiconductor technology data has never before been employed by other applied economists.

In order to test for an association between the level of geographical peripherality and the vintage of technology implemented, we employ both an empirical approach and a diagrammatic approach.

The first part of our analysis is to observe broad scale changes in the spatial evolution of the industry. Figures 2a and 2b describe the 1995 and the 2004 distributions of wafer production lines and R&D plants of semiconductor firms in the US, Figures 3a and 3b describe the 1995 and 2004 distributions of wafer production lines and R&D plants of semiconductor firms in the EU, and Figures 4a and 4b describe the 1995 and 2004 distributions of wafer production lines and R&D plants of semiconductor firms in Asia. The second part of our analysis is to observe changes in the spatial evolution of individual firms within the industry. Here we take four individual cases, and once again we observe the changes over time in their spatial patterns of technological development.



The cases we take are Intel (USA), Texas Instruments (USA), Philips (Netherlands) and Toshiba (Japan). Figures 5a and 5b describe the 1995 and 2004 distributions of wafer production lines and R&D plants of Intel, Figures 6a and 6b describe the 1995 and 2004 distributions of wafer production lines and R&D plants of Texas Instruments, Figures 7a and 7b describe the 1995 and 2004 distributions of wafer production lines and R&D plants of Philips, and finally Figures 8a and 8b describe the 1995 and 2004 distributions of wafer production lines and R&D plants of Toshiba.

In situations such as this where there are multiple pieces of data for each observation, and where observations are produced in very different contexts, a cluster-analysis methodology (Everitt et al. 2001) is often used within social science research. This is a technique which uses linear programming algorithms to group the observations into groupings in which certain types of data outcomes are associated. As such, groupings of characteristics which are relatively correlated with each other are used to classify observations. This allows us to identify distinct groupings of observation types, which share common characteristics, from within a larger sample. Therefore, we first use a cluster-analysis in order to classify all of the individual production lines into four different classes according to their levels of technology, by combining the two production technology indices, namely the minimum processing rule and the wafer size. Secondly, once we have identified the individual clusters, we split these different technology groupings according to the levels of production capacity of each production line, in terms of the total number of 200mm silicon wafers or equivalent which are produced monthly. In each of the following figures, each circle represents an individual production line. The technology class of the production technology is described by the brightness of the black and white colour. The black colour represents the more advanced level of technology and white colour represents the least advanced level. Finally, the level of the production capacity of the production line is described by the size of each circle. In addition, each figure also contains information about the pilot and R&D plants, which are depicted here with squares. These pilot and R&D plants are the plants in which the production line is directly allied to a R&D facility, rather than being simply a dedicated standalone production facility. Once again, the level of technology is depicted using colour shading, and the scale of the R&D facility is depicted according to the size of the square. As we see in the following diagrams, using cluster analysis, the 1995 data produces four distinct groupings of technology, whereas the 2004 data produces five distinct groupings of technology. Group 4 technology, which is the highest level of technology in 1995, corresponds to approximately group 3 technology in 2004, above which there are two new levels. This indicates the level of technological development over this period. These six global-region diagrams and the eight firm diagrams allow us to observe the spatial evolution and the changes in the spatial patterns of technology of both the overall semiconductor manufacturing industry and also individual firms within the industry over the last decade.

### ***5. Analysis and Discussion***

With our technology, plant and spatial data we can now begin to investigate the relationship between geography and the implementation of technology within the wafer

processing component of the semiconductor industry. Following either product-cycle (Vernon 1966), stage theory (Johansson and Vahlne 1977) or orthodox international business arguments (Dunning 1977) applied to either regional (Vernon 1960; Markusen 1985) or international locations (Vernon 1966, 1979; Dunning 1977, 1988, 1992) we can hypothesize that different generations of semiconductor technologies will be spatially differentiated within the semiconductor industry. In particular, on the basis of a simple product life cycle model (Vernon 1960; Markusen 1985) we would expect that the most recently developed products requiring the most advanced, miniaturized and newer production technologies will tend to be implemented in location which are traditionally regarded as being central to the semiconductor industry, such as Silicon Valley, Tokyo, and The Netherlands. On the other hand, more mature vintages of product and process technologies would be expected to be implemented in more geographically peripheral locations exhibiting lower wage rates, relative to these central locations. Such locations would typically be in less-developed lower-wage regions, with the organizational control still being maintained in the advanced central locations. From the product life cycle perspective, the reason for this is that less advanced technology products will have become rather more standardized and therefore easier to mass produce than more recent higher technology products. As such, the human capital inputs required to produce more standardized technologies will be less. Moreover, increasing production quantities also imply the need for larger plants with larger land and labour requirements. In a product cycle framework, the combination of these two effects will therefore provide an incentive for such plants to be located in lower wage, lower skill, and lower land price regions. Although there are both subtle and complex variations in how the international business literature treats geography (McCann and Mudambi 2004, 2005), depending primarily on the treatment of both organizational and transactions-costs issues, the overall relationships concerning the expected pattern of technology and geography can still be summarized by this simple centre-periphery type description. As such, if this argument is correct, then we ought to observe a strong positive correlation between increasingly mature vintages of a technology, the location of the product and process technology implementation, and the level of geographic peripherality of the establishment.

We recall from our above description of technology indices, that the more advanced generations of technology are represented either by smaller minimum processing rules or by larger wafer sizes. Therefore, using this information, it should be possible to identify the extent to which these simple product life cycle arguments hold. If the product life cycle arguments described here hold, then we would expect that core advanced technologies will be being produced in central core locations, while more basic mature vintage technologies will be being produced in more geographically peripheral locations.

If we consider Figures 2a and 2b, which describe the 1995 and the 2004 distributions of wafer production lines and R&D plants of semiconductor firms in the US, Figures 3a and 3b, which describe the 1995 and 2004 distributions of wafer production lines and R&D plants of semiconductor firms in the EU, and Figures 4a and 4b, which describe the 1995 and 2004 distributions of wafer production lines and R&D plants of semiconductor firms in Asia, we see that there is very little evidence of any simple overall global centre-periphery geography within the semiconductor industry. In particular, the although US is

the origin of many of the early innovations and technological developments within the industry, over the period 1995 to 2004 the relative contribution of both R&D and also wafer production of both the EU and Asia to the global semiconductor industry has increased significantly, and the relative dominance of the US appears to have disappeared. As such, there is no consistent simple centre-periphery logic to the industry on a global scale.

At the same time, there have also been some significant changes in the contribution and distribution of activities even within each of these three super global-regions. In the case of the US, we see from Figures 2a and 2b that the production capacity, the levels of technology, and the R&D capacity of the EU semiconductor industry have all increased significantly over the period 1995-2004. During this time, since 1995 there has been a relative shift away from the dominance of the West Coast. Although places such as Silicon Valley, California, Oregon, Texas and New York State still seem to be core places in terms of the industry's sub-regional clusters, other areas have also developed. In particular, areas in the non-coastal Western states appear to have grown in importance, along with many of the North Eastern states, while the industry has almost no presence in the mid-Western states. In addition, there has been something of a qualitative shift in the distribution of technologies, in that these more newly-emerging states are the ones which combine both concentrations of production lines along with lines of the latest technology. California is therefore no longer dominant in these technologies.

If we consider Figures 3a and 3b, which describe the 1995 and 2004 distributions of wafer production lines and R&D plants of semiconductor firms in the EU, we see that the production capacity, the levels of technology, and the R&D capacity of the EU semiconductor industry have all increased significantly over the period. As such, these features are similar to the case of the US. In addition, as with the case of the US, there has also been something of a shift in the relative contribution and distribution of activities even within European super-region. In particular, there has been a general steady drift eastwards of many semiconductor activities, whereby EU semiconductor producers have invested in production facilities and in some limited R&D facilities in former transition and communist countries. Importantly, however, in the case of many of these Eastern European investments, although they are still relatively small in comparison with those located in Western Europe, they are in relatively new technologies, and not in old or mature vintage technologies.

From Figures 4a and 4b, which describe the 1995 and 2004 distributions of wafer production lines and R&D plants of semiconductor firms in Asia, we see that the production capacity, the levels of technology, and the R&D capacity of the Asian semiconductor industry have all increased very significantly over this period. As such, these features are similar to the cases of both the US and the EU. Once again, and similar again to the case of both the US and the EU, there has also been something of a shift in the relative contribution and distribution of activities even within East Asian super-region. In particular, while Japan remains very strong in the semiconductor industry, as was mentioned earlier, firstly Taiwan and secondly South Korea have both recently emerged as very significant global industry players, with enormous R&D capabilities, as well as

very high levels of production capacity (*Business Week* 2005).

While these figures indicate that there has been a general geographical spreading of the global semiconductor industry, our analysis also demonstrates that there is no simple or consistent centre-periphery logic to the industry on a global scale, of a type implied by product cycle arguments (Markusen 1985). On the contrary, the locations' characteristics of the semiconductor production lines and R&D facilities are heterogeneous and no clear association can be observed between the level of geographical peripherality and the vintage of technology implemented. Therefore, it may be that the spatial patterns of technological implementation within the semiconductor industry are determined primarily by factors which are not included in orthodox product-cycle type specification, and such factors may include organizational and transactions-costs issues. Following this argument, a possible alternative explanation for our lack of support for the product-cycle model within the global semiconductor industry is that the wafer processing activities of the industry is comprised almost entirely of plants which are part of vertically-integrated hierarchical organizations, and the relationship between technology and geography in this industry depends on the spatial organization of these vertically-integrated firm hierarchies. These are points that we will now consider with the help of Figures 5a to 8b, which provide details as to the location of the semiconductor wafer manufacturing R&D and production facilities of four major global semiconductor producers, namely Intel, Texas Instruments, Royal Philips Electronics Semiconductor, and Toshiba. These diagrams allow us to observe how these firms have developed their spatial patterns of activities over time, and therefore to consider the types or organizational or transactions costs issues which may be pertinent to their spatial organizational behaviour.

Figures 5a and 5b provide us with information about the geographical organization of Intel. Intel is a dedicated semiconductor microchip firm based in Silicon Valley, and as we see in Figures 5a and 5b, within the US Intel has several plants undertaking combined semiconductor R&D and wafer-processing activities in the area surrounding the Silicon Valley location of its headquarters, as well as similar facilities in Oregon. In addition, Intel also has wafer manufacturing facilities in South Western states of Arizona and New Mexico. Over the last decade, however, Intel has rationalized the number of its combined R&D and production facilities on the West Coast, while at the same time slightly increasing the number of its wafer manufacturing facilities in other US states outside of either the South West or the West Coast. In terms of international investments, Intel has retrenched over the last decade, in the sense that as well closing its Japanese operations, its remaining overseas investments no longer produce the most advanced levels of technologies, as was the case in 1995.

Figures 6a and 6b provide us with information about the geographical organization of Texas Instruments. Texas Instruments is a multi-product electronics firm, of which one of its major activities is the production of wafers and microchips. From a spatial perspective, Texas Instruments is a much more tightly controlled organization than Intel, in that all of its domestic semiconductor wafer production and R&D facilities are within the state of Texas, and this has continued to be the case over the last decade. In terms of overseas investment, as with Intel, Texas Instruments has slightly retrenched its activities, in that

as well closing its Italian operations, none its remaining overseas investments produce the most advanced levels of technologies, as was the case in 1995.

The spatial-organizational patterns of both Intel and Texas Instruments are similar to the spatial investment patterns of other US vertically integrated semiconductor producers such as Motorola, National Semiconductor and Advanced Micro Devices (Arita and Fujita, 2001; Arita and McCann 2002a,b,c; 2004, 2006). Within these US firms, there are often a large number of locations undertaking semiconductor production activities. Almost all of these activities are either in combined R&D and wafer-processing activities, i.e., the first and second stages of the production process, or only in the wafer processing activities, i.e. in the second stage of the production process. These activities are often clustered together around the headquarters locations of the companies, but such clusters are not necessarily exclusively in these areas. Moreover, within the US, not all plants are located in spatial clusters, but are often individually sited in a range of locations. Whether or not a firm has an R&D facility in Silicon Valley depends largely on the founding location of the firm. In terms of the overseas operations of the US firms, significant proportions of their wafer-processing activities, as well as all of their wafer assembly activities, take place outside of the US. However, the evidence here, suggests that the period 1995-2004 has been somewhat a period of international retrenchment for the overseas operations of the US semiconductor producers.

Figures 7a and 7b provide us with information about the geographical organization of Royal Philips Electronics Semiconductor, one of the product divisions of Royal Philips Electronics based in Amsterdam and Eindhoven, The Netherlands. As we see, Philips has expanded its semiconductor activities significantly over the decade 1995-2004, although it has tended to keep all these activities within a close geographical range of its headquarters locations. For comparison purposes, its plants are only slightly more geographically spread out than those of Texas Instruments, and much less geographically spread out than those of Intel. As Philips has maintained a comprehensive of products including analog and discrete devices used for consumer electronics products, in comparison to the US firms, it has tended to concentrate relatively more on the wafer processing activities, i.e. the second stage of the semiconductor manufacturing process, and relatively less on the first stage. In addition, none of its technology even in Europe is of the very highest level. This is also true of its overseas operations outside of Europe. Moreover, as with Intel and Texas Instruments, Philips has slightly retrenched its activities in that it has closed many of its US and Asian operations, and concentrated them into an individual US facility and an individual Asian facility. As with its European operations, none of Philips remaining overseas investments produce the most advanced levels of technologies. As such, within the global semiconductor industry as a whole, Philips has tended to develop a niche primarily as a mid-range technology manufacturer. The general pattern described in this example of Philips is also broadly replicated in the cases of other major European vertically integrated semiconductor firms such as STMicroelectronics and Infineon Technologies AG.

Figures 8a and 8b provide us with information about the geographical organization of the semiconductor activities of Toshiba, a multi-product Japanese electronics producer. In the

case of Toshiba, there are combined R&D and production facilities in the Tokyo region, plus some smaller such facilities in both the north and the south of Japan. A casual observation of these figures may lead us to conclude that there is an obvious centre-periphery logic to these arrangements. However, while the details of this argument are beyond the scope of this chapter, a close inspection of the organizational aspects of these Japanese firms (Arita and McCann 2002a,b,c; 2006) suggests that these groupings of plants are organized as standalone product-technology divisions within the overall corporate structure, and that this arrangement is designed specifically to avoid the problem of unintended knowledge outflows. As such, this can be shown to be a very different spatial-organizational logic than might be inferred from orthodox models of agglomeration.

The location behaviour of these global semiconductor firms can only be understood as being indicative of traditional multiplant location considerations, as long as we also understand that issues of knowledge capabilities, knowledge control, and the relationship between these knowledge management issues and firm structure are paramount. The traditional multiplant considerations suggest that the location decisions regarding the siting of facilities is based on orthodox multiplant–multinational lines, in which access to a suitable local labour and land is a major consideration, subject to the location of suppliers and customers. In the simple product cycle model (Markusen 1985) there develops a core-periphery logic to the pattern of activities. Moreover, the more recent literature also emphasizes the agglomeration-clustering behaviour of such firms, in order to gain access to knowledge inputs. However, the knowledge management aspects of this industry appear to be entirely different to the simple stylized knowledge access and knowledge management assumptions embedded in the product cycle literature (Markusen 1985) or much of the clustering literature. For example, while the parent and headquarter locations tend to dominate the R&D activities of these firms, these areas are not the only areas in which such R&D activities are located. Nor are the areas immediately adjacent to the parent company headquarters necessarily engaged in higher level operations than the more geographically distant facilities, at least for facilities located within the same global region. Moreover, while each of these firms described here has a tendency to group plants geographically, each of these firms also has a tendency not to locate its plants immediately adjacent to those of its competitors. There are good reasons for this behaviour. The semiconductor manufacturing industry is a very knowledge-intensive industry, and both access to knowledge and retention of knowledge are crucial issues. The location behaviour of firms in general can be shown to depend on the balance between the effective management and control of knowledge inflows and knowledge outflows, and in particular, of unintended knowledge inflows and outflows (McCann and Mudambi 2004, 2005). Moreover, this balance itself can also be shown to depend on the industrial structure. In oligopolistic knowledge intensive industries such as the global semiconductor industry, simple agglomeration-clustering will generally not take place. This is why semiconductor firms are often organized geographically into groups of plants within the same firm, but in locations which are quite different to those of their major competitors, as is the case here. The only real exception to these circumstances is where the organizational boundaries are so extremely tight and clearly defined (McCann and Mudambi 2004, 2005) that no unintended outward knowledge spillovers are possible, in

which case such firms become ‘islands of innovation’ (Simmie 1998).

## ***6. Conclusions***

This paper has discussed the various sub-sectors of the semiconductor industry, and applied a simple product-cycle model to the case of the wafer-processing part of the industry. The data we employ is some of the most detailed and disaggregated technological data available for such an industry. A notable development within the industry over the last decade has been primarily the rise of Asia as a leading centre for the semiconductor industry, followed secondly by Europe, rather than continuing relative dominance of the US. Meanwhile, at the individual firm level, there is some evidence for industrial clustering between among local establishments, but this generally takes place within a tight organizational logic (Arita and McCann 2002a,b,c; 2006) designed specifically to rule out unintended knowledge outflows (McCann and Mudambi 2004, 2005). Overall, our analysis therefore finds little or no support for a simple product cycle type of description of the relationship between the implementation of technological innovations and the location of the activity, either at the international level, or at the level of the individual firm. This is because the technology and knowledge management assumptions embedded in the product cycle model are not appropriate for this industry. The reason is that the spatial patterns of production within the semiconductor industry are dominated by issues of decision-making and control within complex vertically-integrated hierarchical organizations, and these cannot be analysed by adopting a product cycle approach. Rather, we would argue that a much more sophisticated analysis involving industry structure and transactions costs is required in order to understand the geographical organization of this industry. By adopting such an approach, it can be shown that our observations here are consistent with an analytical framework in which activities are spatially differentiated across local labour markets according to the skill requirements of the firms’ various activities and operations, the available land and human capital inputs available at particular locations, and the locations of the markets and inputs supplied for the plants, as long as we also acknowledge the extent to which such firms will wish to avoid unintended outward knowledge spillovers.

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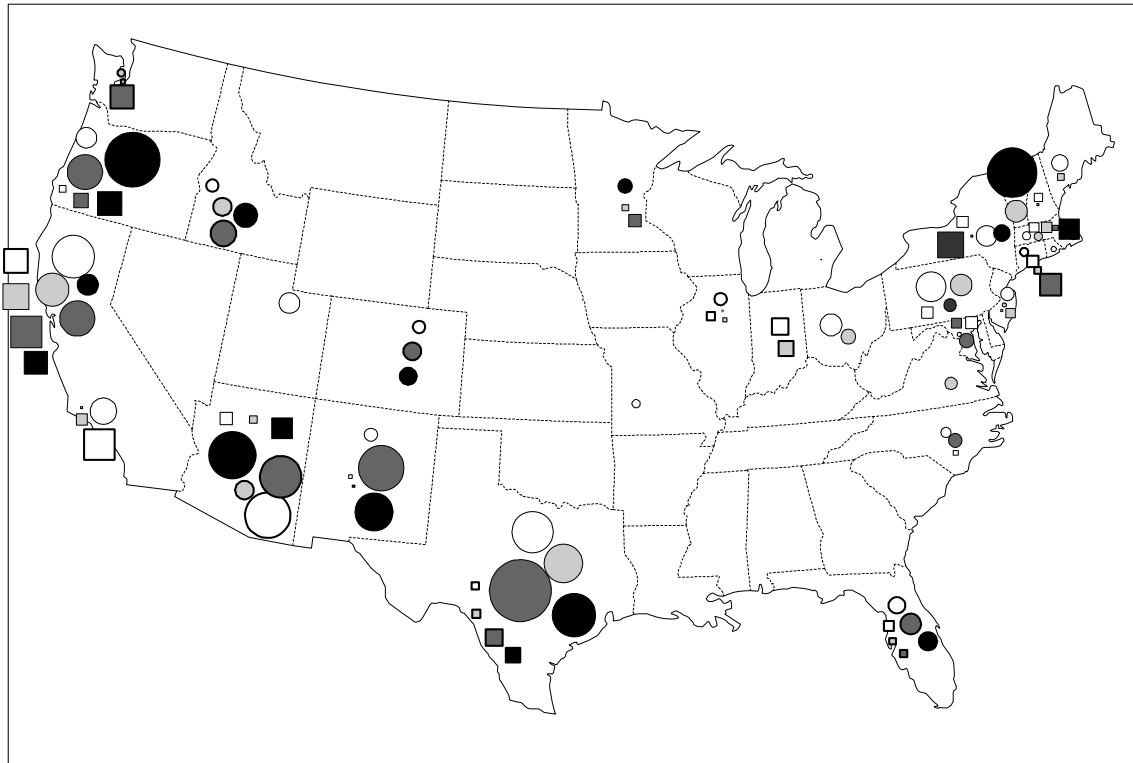
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**Production Process of Semiconductor  
Comparison with Publishing and Printing**

<b>Semiconductor</b>		<b>Books</b>	
<b>DESIGN</b>	Planning & Design of Circuits	Planning & Editing of Manuscript	<b>PUBLISHING</b>
	Layout Design Mask Making	Layout Block Copy	
<b>WAFER PROCESS</b>	Lithography	Plate Making Phototype Process	<b>PRINTING</b>
	Wafer Manufacturing Process	Printing	
<b>ASSEMBLY</b>	Assembly	Book-binding	<b>BOOK-BINDING</b>
	Testing	Testing	
	Silicon Wafer (Wafer Manufacturing Makers)	Papers (Paper Manufacturing Makers)	

**Figure 1.** Production Process of semiconductor: comparison with book publishing and printing

**Figure 2a.** US Semiconductor Plants: Distribution of Wafer Production Lines 1995



US Semiconductor Plants  
Distribution of Wafer Production Lines  
1995

■ R&D, Pilot Plant  
● Wafer Plant

○ Technology Rank 1:Lowest  
 ◐ Technology Rank 2:Lower  
 ◑ Technology Rank 3:Higher  
 ● Technology Rank 4:Highest

The gradations of the black-white colors represents the level of production technologies in the wafer production lines

○ 50,000 6-inch wafers processed per month  
 ○ 100,000 6-inch wafers processed per month

The area of each circle /square represents the production capacity in terms of the number of 6-inch wafer processed per month (aggregated amount per state (except CA and Silicon Valley area))

**Figure 2b. US Semiconductor Plants: Distribution of Wafer Production Lines 2004**



**US Semiconductor Plants  
Distribution of Wafer Production Lines  
2004**

■ R&D, Pilot Plant  
● Wafer Plant

○ Technology Rank 1:Lowest  
 ◐ Technology Rank 2:Lower  
 ◑ Technology Rank 3:Middle  
 ◒ Technology Rank 4:Higher  
 ● Technology Rank 5:Highest

The gradations of the black-white colors represents the level of production technologies in the wafer production lines

○ 50,000 6-inch wafers processed per month  
 ○ 100,000 6-inch wafers processed per month

The area of each circle /square represents the production capacity in terms of the number of 6-inch wafer processed per month (aggregated amount per state (except CA and Silicon Valley area))

**Figure 3a. EU Semiconductor Plants: Distribution of Wafer Production Lines 1995**



**EU Semiconductor Plants  
Distribution of Wafer Production Lines  
1995**

■ R&D,Pilot Plant  
● Wafer Plant

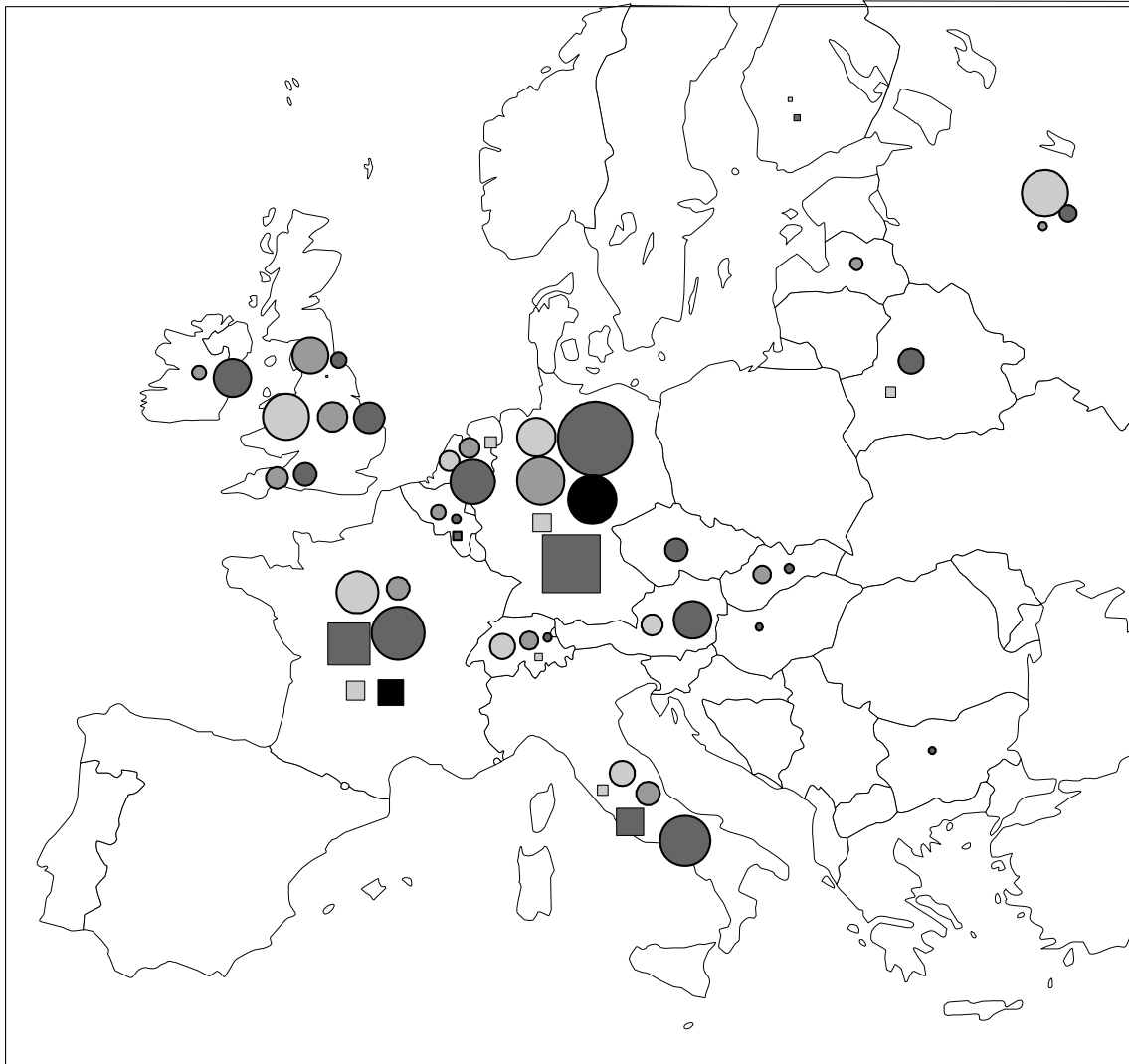
○ Technology Rank 1:Lowest  
 ◐ Technology Rank 2:Lower  
 ◑ Technology Rank 3:Higher  
 ● Technology Rank 4:Highest

The gradations of the black-white colors represents the level of production technologies in the wafer production lines

○ 50,000 6-inch wafers processed per month  
 ○ 100,000 6-inch wafers processed per month

The area of each circle /square represents the production capacity in terms of the number of 6-inch wafer processed per month (aggregated amount per country)

**Figure 3b. EU Semiconductor Plants: Distribution of Wafer Production Lines 2004**



**EU Semiconductor Plants  
Distribution of Wafer Production Lines  
2004**

■ R&D, Pilot Plant  
● Wafer Plant

○ Technology Rank 1:Lowest  
 ○ Technology Rank 2:Lower  
 ○ Technology Rank 3:Middle  
 ○ Technology Rank 4:Higher  
 ○ Technology Rank 5:Highest

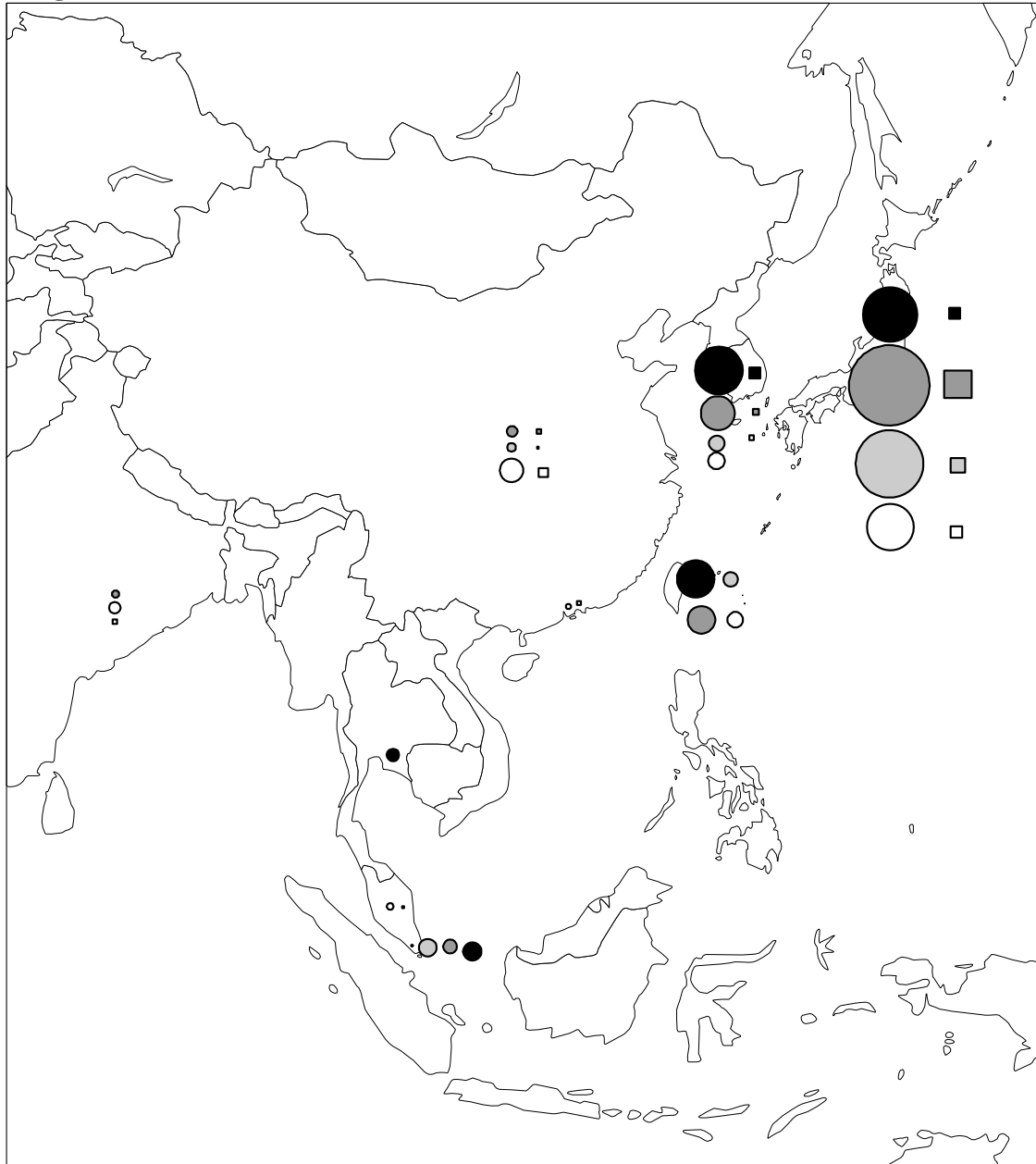
The gradations of the black-white colors represents the level of production technologies in the wafer production lines

○ 50,000 6-inch wafers processed per month  
 ○ 100,000 6-inch wafers processed per month

The area of each circle /square represents the production capacity in terms of the number of 6-inch wafer processed per month (aggregated amount per country)



**Figure 4a.** Asia Semiconductor Plants: Distribution of Wafer Production Lines 1995



**Asia Semiconductor Plants  
Distribution of Wafer Production Lines  
1995**

■ R&D, Pilot Plant  
● Wafer Plant

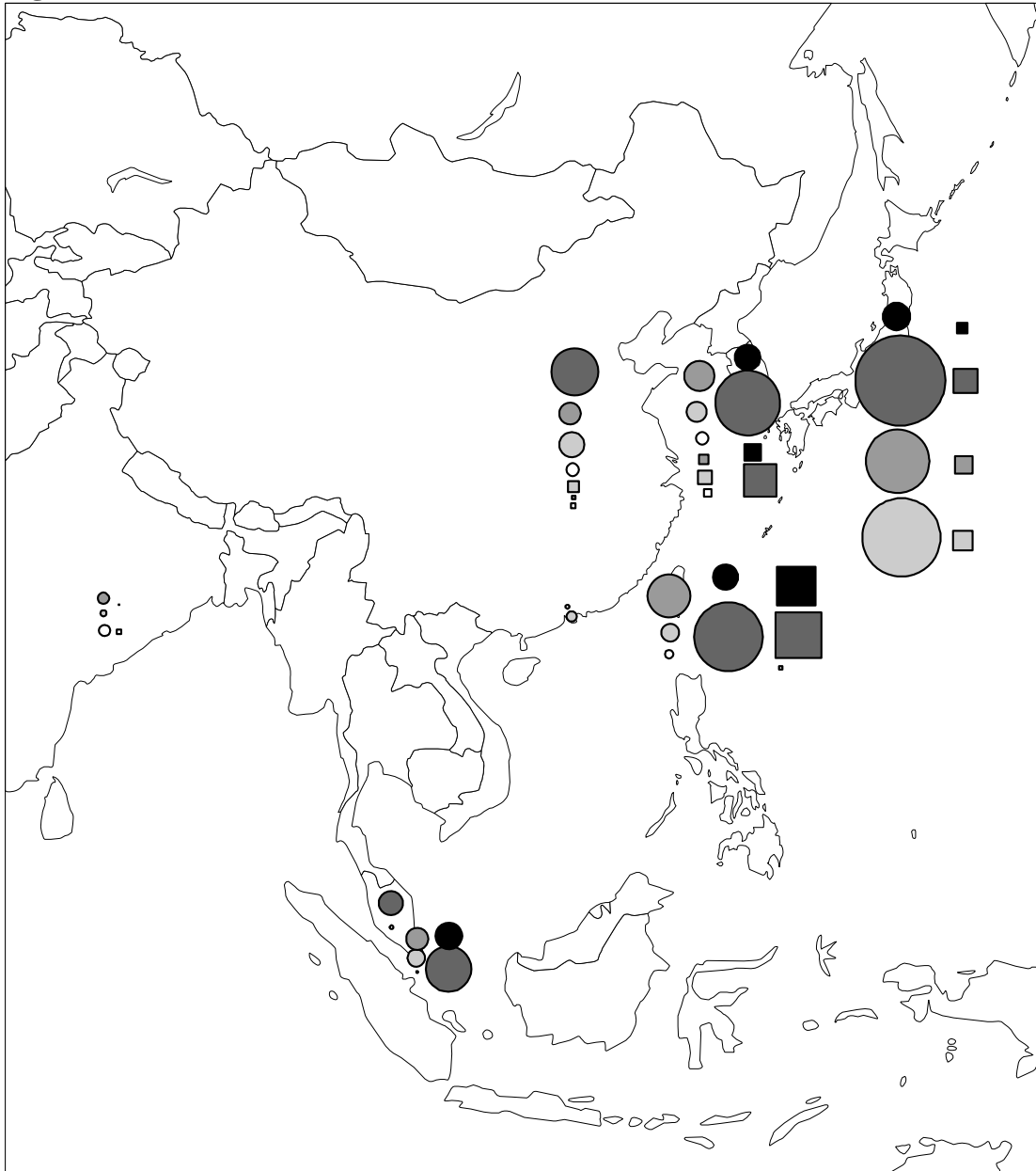
○ Technology Rank 1: Lowest  
 ◐ Technology Rank 2: Lower  
 ◑ Technology Rank 3: Higher  
 ● Technology Rank 4: Highest

The gradations of the black-white colors represents the level of production technologies in the wafer production lines

○ 100,000 6-inch wafers processed per month  
 ○ 500,000 6-inch wafers processed per month

The area of each circle /square represents the production capacity in terms of the number of 6-inch wafer processed per month (aggregated amount per country)

**Figure 4b.** Asia Semiconductor Plants: Distribution of Wafer Production Lines 2004



**Asia Semiconductor Plants  
Distribution of Wafer Production Lines  
2004**

■ R&D, Pilot Plant  
● Wafer Plant

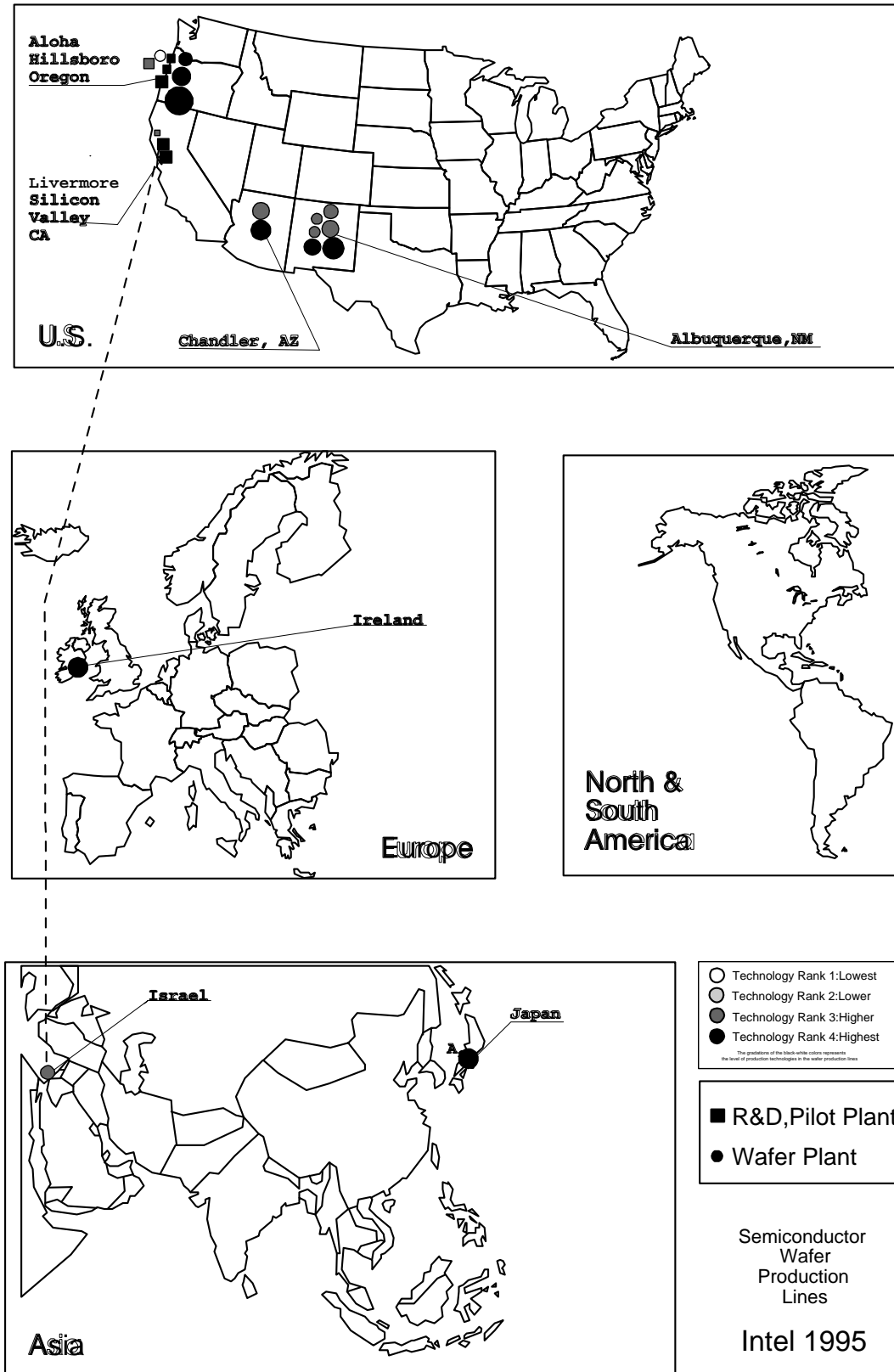
○ Technology Rank 1:Lowest  
 ◐ Technology Rank 2:Lower  
 ◑ Technology Rank 3:Middle  
 ◒ Technology Rank 4:Higher  
 ● Technology Rank 5:Highest

The gradations of the black-white colors represents the level of production technologies in the wafer production lines

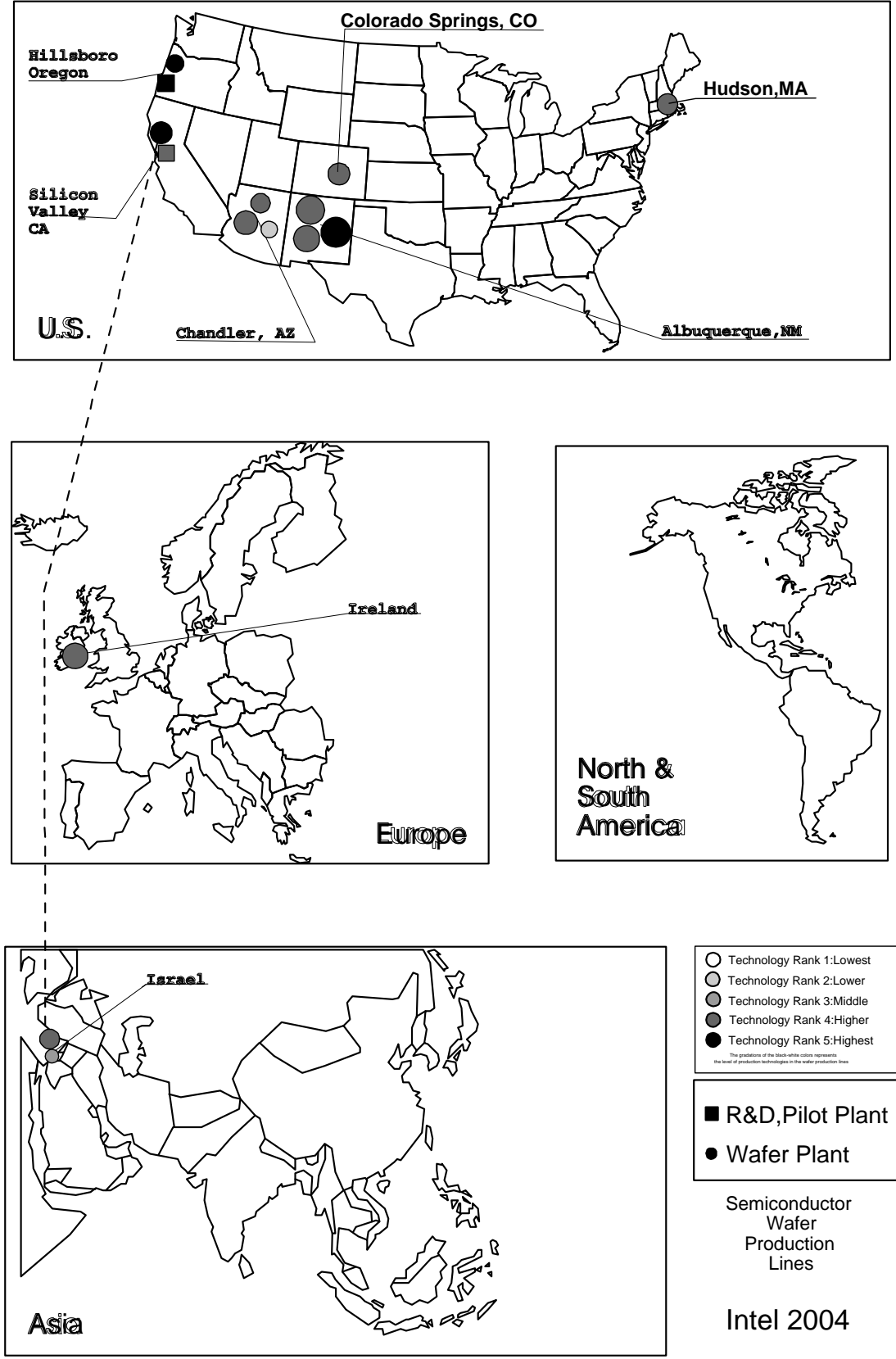
○ 100,000 6-inch wafers processed per month  
 ○ 500,000 6-inch wafers processed per month

The area of each circle /square represents the production capacity in terms of the number of 6-inch wafer processed per month (aggregated amount per country)

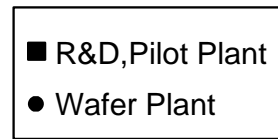
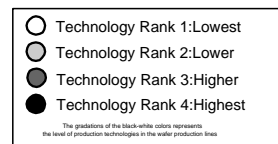
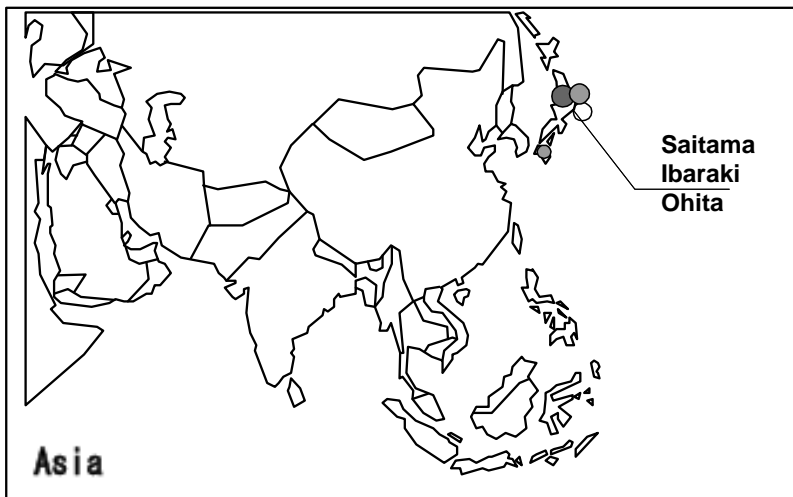
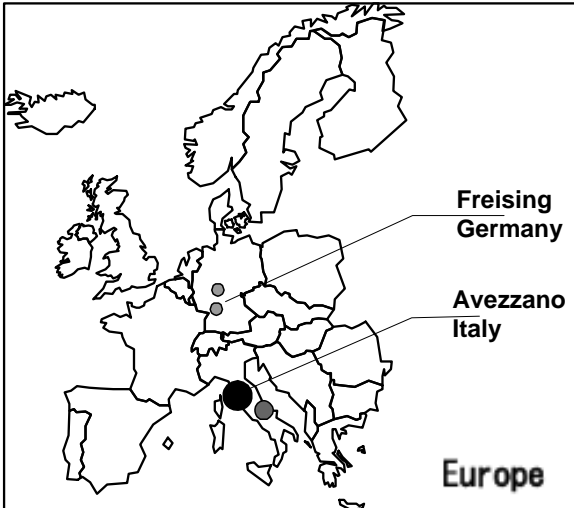
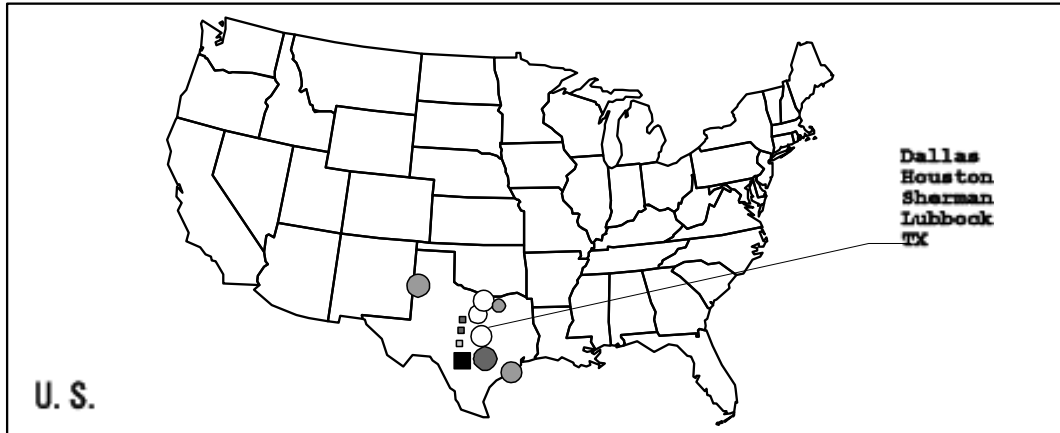
Figure 5a. Semiconductor Wafer Production Lines: Intel 1995



**Figure 5b. Semiconductor Production Lines: Intel 2004**

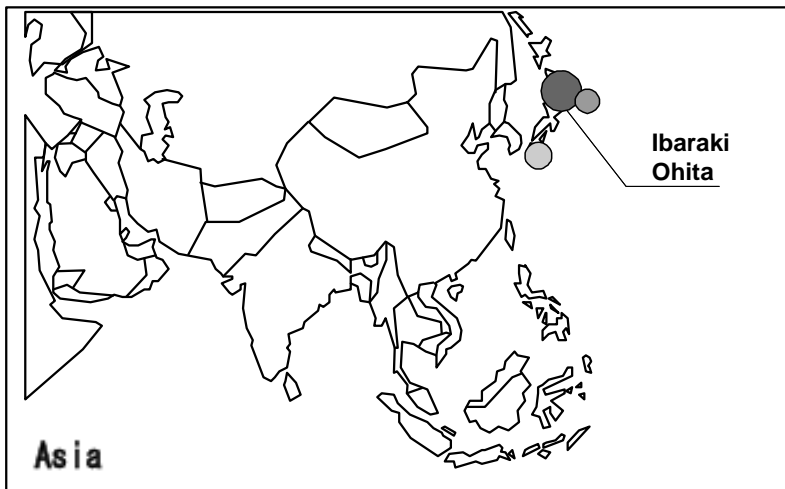
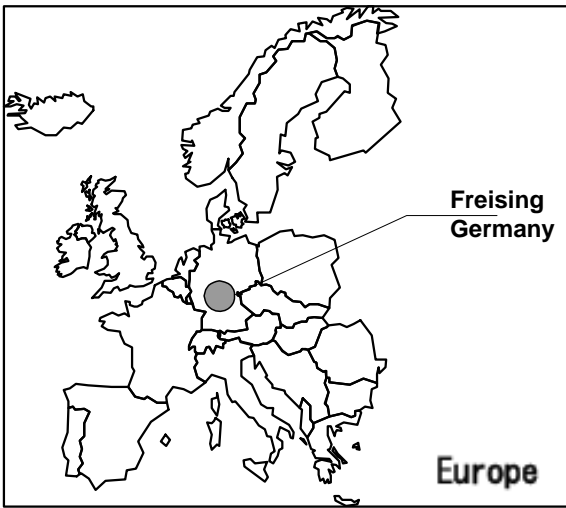
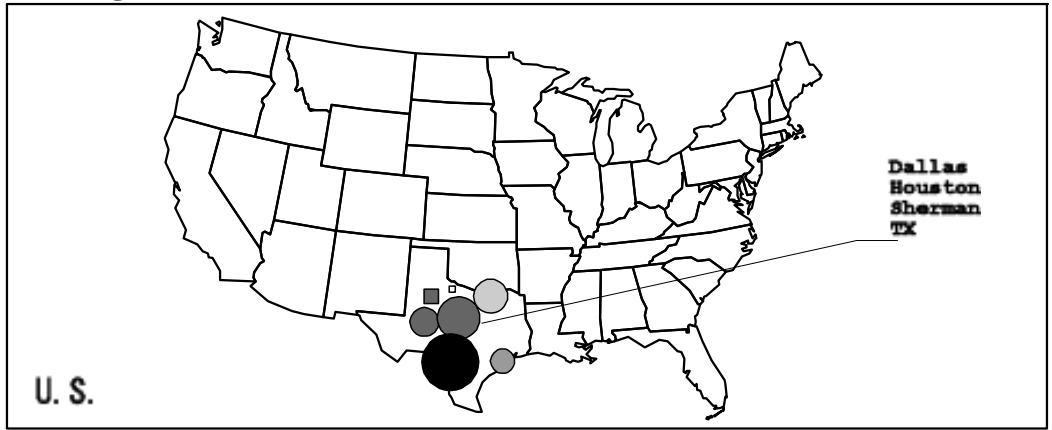


**Figure 5a. Semiconductor Wafer Production Lines: Texas Instruments 1995**



Semiconductor  
Wafer Production Lines  
Texas Instruments  
1995

**Figure 5b. Semiconductor Wafer Production Lines: Texas Instruments 2004**

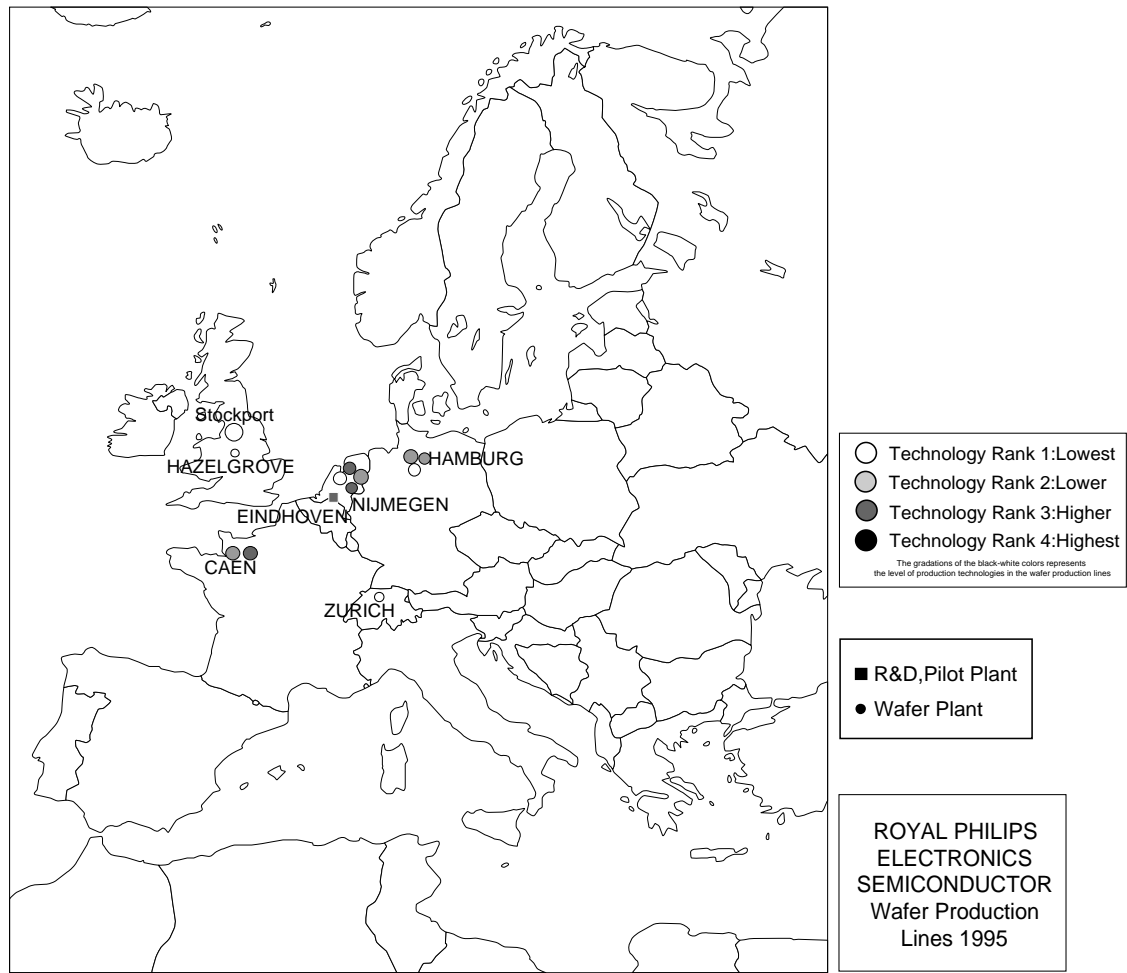


- Technology Rank 1:Lowest
  - Technology Rank 2:Lower
  - Technology Rank 3:Middle
  - Technology Rank 4:Higher
  - Technology Rank 5:Highest
- The gradations of the black-white colors represents the level of production technologies in the wafer production lines.

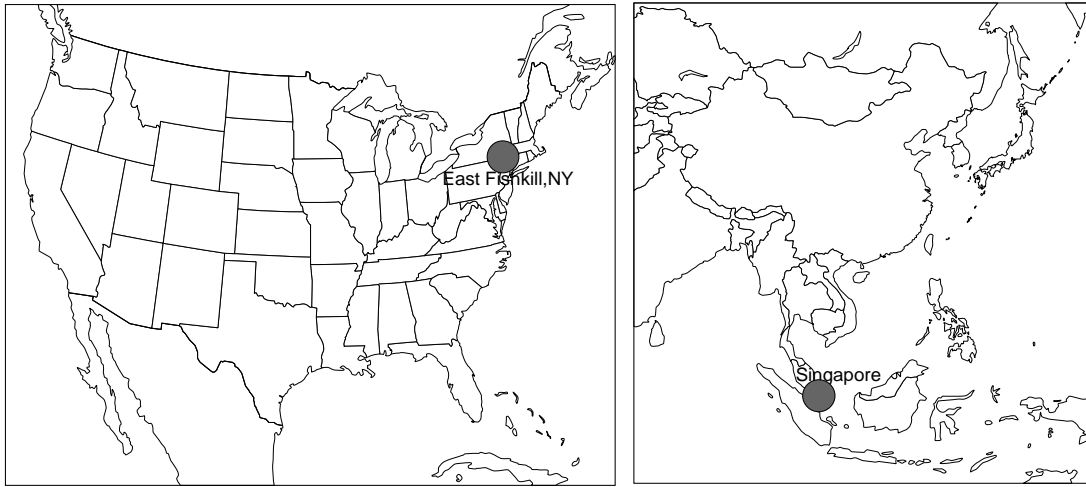
- R&D,Pilot Plant
- Wafer Plant

Semiconductor  
Wafer Production Lines  
Texas Instruments  
2004

**Figure 6a.** Semiconductor Wafer Production Lines: Philips Electronics 1995

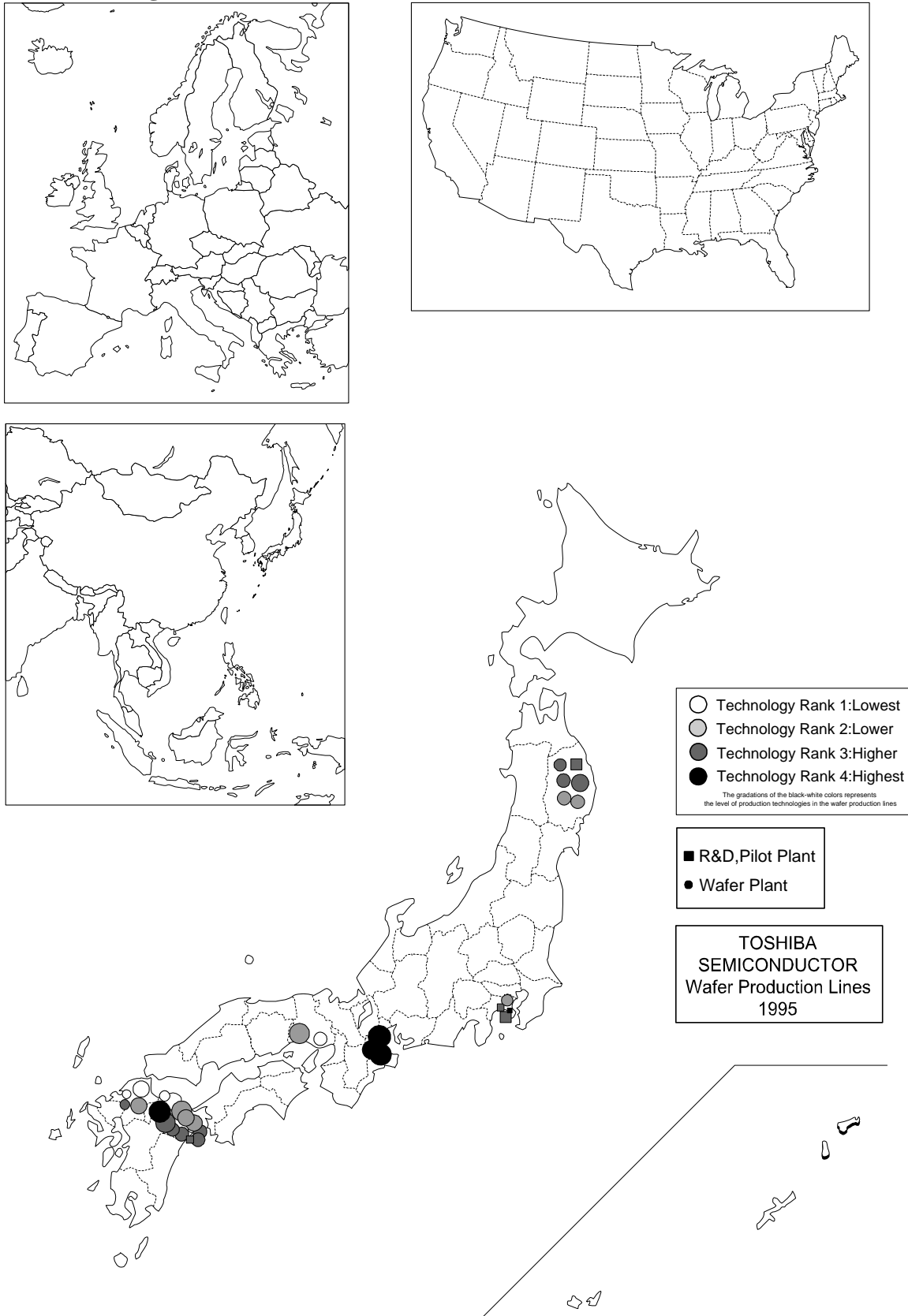


**Figure 6b. Semiconductor Wafer Production Lines: Philips Electronics 2004**





**Figure 7a. Semiconductor Wafer Production Lines: Toshiba 1995**



**Figure 7b. Semiconductor Wafer Production Lines: Toshiba 2004**

